A novel hybrid topology for power quality improvement using multilevel inverter for the reduction of vibration and noise in brushless DC motor for industrial applications

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Abstract. The proposed research involves the design and implementation of a novel hybrid Topology for Power Quality Improvement using Multilevel Inverter to reduce vibration and noise in BLDC motor for industrial applications. The utility of power electronics device plays a vital role for various applications in recent days. Similarly, the power consumption is also important for all processing units. The power electronic devices contain a lot of converters for processing the energy. During such cases, the harmonics are produced in different ways. Hence, a system analysis is necessary to find the problem at conventional methods. Hence the problem is identified on the distribution static compensator (DSTATCOM) component module whose harmonics are high, and it is important module for the circuit, hence preventive action to be taken to reduce the harmonics. To limit or reduce the harmonics, it is required to modify the triggering mechanism and control unit of Multi level inverter. Hence, the proposed hybrid method is implemented with the developed H-bridge and diode clamped topology with a brushless dc motor. In addition, the vibrations and the noise level are also reduced due to the reduced total harmonic distortion. The proposed module is simulated on MATLAB Simulink, and an experimental analysis is carried out to verify functionality tools with various operating conditions, the proposed method proves more efficient than the switches and complex networks present in traditional methods.

Keywords: Buck-boost Cuk converter, BLDC motor, solar array, PWM inverter, wind energy, vibration, noise, battery.

1. Introduction

With the advancing deregulation of the electric utility industry, different changes are always recognized. Since, the power is continuously considered as a thing, transmission systems are pushed closer to their quality and warm purposes of limitation, while the accentuation on the idea of vitality became huger than in another time. In the deregulated utility condition, money-related and promotion powers will continue to ask for a more perfect and productive task of the power framework regarding age, transmission, and circulation. Presently, like never before, cutting edge advancements are foremost for the strong and secure task of energy systems. Power electronic based equipment such as Flexible AC Transmission Systems (FACTS), High-Voltage DC (HVDC), and Custom Power advancements constitute a segment of the most encouraging particular movements to address the new working challenges being displayed today. These degrees of progress rely upon a better limit of vitality electronic apparatus in order to quickly react to framework occasions. So, the increment control exchange restricts and enhances the nature of energy conveyed. In the past couple of years, the high-power applications are leading the world with the respect of their wide expanding consideration. Since, numerous topologies, strategies and drive applications are reviewed and discussed. Such converters are reasonable with high power

devices based on their rating. Reference [1, 2] framed the multilevel power conversion topology with neutral point clamped topology. Recent days, the demand in electronics devices was associated with many fast charging devices which external energy sources require early investigation on harmonic and non-active power compensation [3, 4]. This widespread harmonic polluting device both reduces the system efficiency and has detrimental impacts on grid voltage distortion levels [5]. Hence, the addition of current leads to heat losses and creates some issues in sensitive electrical devices. Some recent researchers are focused on power quality issues and current harmonics. Power Quality is the way to effective conveyance of quality item and the activity of an industry. It is presently significantly more basic for the business on account of expanding use of electronic loads and electronic controllers which are complex to the nature of energy provided. The expanding emphasis on the general power framework effectiveness brought about the utilization of devices such as high effectiveness, flexible speed engine drives and shunt capacitors for control factor remedy to decrease losses bringing about expanding consonant levels on control frameworks. For various applications like agricultural and industrial different topologies of power-controlled devices are designed to embed with the renewable resources. Henceforth Multilevel inverters (MLIs) are growing as a current scientific thing of power-controlled devices for high-power applications [6]. Power-controlled devices clamped multilevel inverter (PMLI), soaring capacitor MLI (SCMLI) and multilevel inverter which is cascaded (CMLI) are the three major parameters of MLI [7]. CMLI creates the stepped alternating current pulses with additional DC power with compact oscillations content [8]. It acts as an extra gorgeous topology compared to other two topology. Conventional Cascaded Multilevel inverter (CCMLI) is shown in Fig. 1.

The structure is reconstructed with three renewable sources with a permanent magnet brushless DC motor. Cascaded Multilevel inverter with BLDC motor (CMLIBLDC) is shown in Fig. 2.

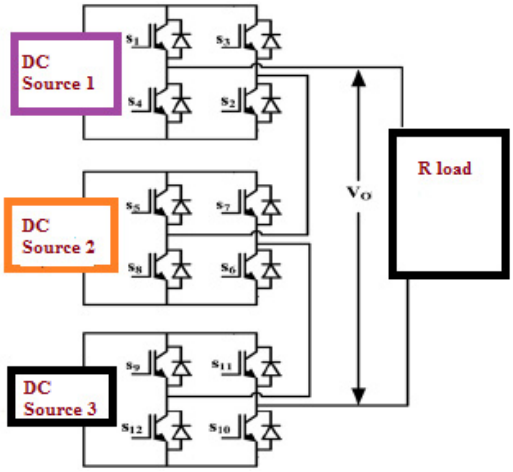


Fig. 1. Schematic circuit diagram of CCMLI

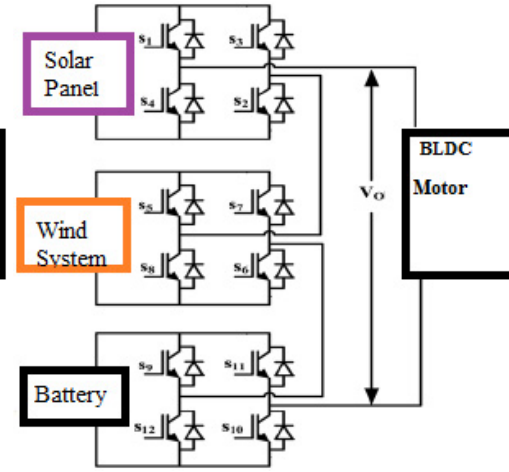


Fig. 2. Schematic circuit diagram of (CMLIBLDC)

For obtaining output nominal in CCMLI, new topology, such as multilevel converter topology is proposed between the various input sources moreover considering transformer. An effective use of CCMLI, buck-boost Cuk cascaded multilevel inverter (BBCCMLI) topology modifications is despoiled due to the lot of power controlled devices and Direct current power. The proposed cascaded DC link circuit diagram is shown in Fig. 3.

Meanwhile topological alterations are made in the existing CCMLI [9-13]. Henceforth in proposed research, the two buck-boost converter circuit is introduced between input sources and DC-link inverter to obtain nominal output voltage. The input DC voltage is highly energized toward desired potential level through BB Cuk converter system. Such modifications of topology results in the reduction of power controlled devices and input sources. For this research, a

single-phase thirty-one-stage asymmetrical power DC-DC Cuk linking direct current cascaded multilevel CMLI (BBCDCLCMLI) network is designed for industrial and agricultural Usages. Schematic circuit of the designed BBCDCLCMLI structure is given on Fig. 4.

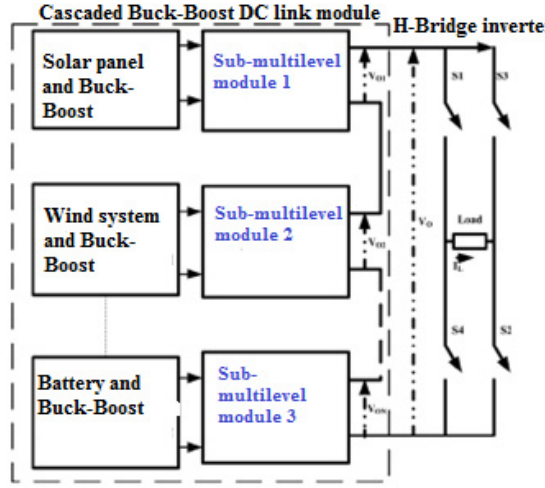


Fig. 3. Proposed schematic diagram of DC-DC Cascaded DC-link Multilevel inverter

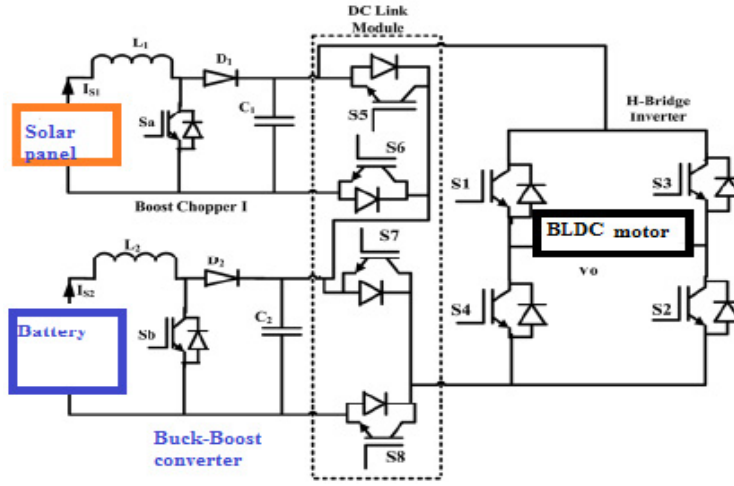


Fig. 4. Proposed circuit diagram of BBCDCLCMLI with BLDC motor

Achieving improved superiority of AC power (by reducing oscillations on converter), to get sinusoidal wave a multicarrier pulse width modulation is proposed accordingly power-controlled device topology is intended to linking direct current controlled devices [14-17]. The improved PSO algorithm is used to optimize the parameters of least squares support vector machines (LS-SVM) in order to construct an optimal LS-SVM classifier, which is used to classify the fault. Finally, the proposed fault diagnosis method is fully evaluated by experiments and comparative studies for motor bearing for reduction of vibration [18]. Another algorithm MGACACO is proposed makes use of the exploration capability of GA and stochastic capability of ACO algorithm. In the proposed MGACACO algorithm, the multi-population strategy is used to realize the information exchange and cooperation among the various populations. The chaotic optimization method is used to overcome long search time, avoid falling into the local extremum and improve the search accuracy [19]. A vibration signal analysis method is the most popular technique that is used to monitor and diagnose the fault of motor bearing. However, the application

of the vibration signal analysis method for motor bearing is very limited in engineering practice. In this paper, on the basis of comparing fault feature extraction by using empirical wavelet transform (EWT) and Hilbert transform with the theoretical calculation, a new motor bearing fault diagnosis method based on integrating EWT, fuzzy entropy, and support vector machine (SVM) called EWTFSFD is proposed. In the proposed method, a novel signal processing method called EWT is used to decompose vibration signal into multiple components in order to extract a series of amplitude modulated-frequency modulated (AM-FM) components with supporting Fourier spectrum under an orthogonal basis is proposed [20]. The vibration signal of motors under no-load and load states are used to testify the effectiveness of the proposed HMGSEDI method. The experiment shows that high-order differential mathematical morphology entropy can more effectively identify the fault damage degree of bearings and the identification accuracy of fault damage degree can be greatly improved. Therefore, the HMGSEDI method is an effective quantitative fault damage degree identification method and provides a new way to identify fault damage degree and fault prediction of rotating machinery are proposed [21]. The new algorithm is proposed on the reduction of vibration on motor [22]. Another approach, the Alpha-stable distribution theory is used to replace the uniform distribution in order to escape from the local minima in a certain probability and improve the global search ability. Next, the DOADAPO algorithm is used to solve the constructed multi-objective optimization model of gate assignment in order to fast and effectively assign the gates to different flights in different time [23].

2. Materials and methods

BBCDCLMLI contains dual unbalanced Direct current power, DC-DC Cuk converter unit, linking voltage DC and hybrid topology. Hybrid topologies are connected parallel on dc-link network.

2.1. DC-link configuration on improved converter

BBC converter element are connected in unbalanced power sources, additionally DCLM has dual MOSFET switch whose output is always in one direction. Fig. 4 shows the Corresponding schematic circuit of BDCLMLI.

BDCLMLI configuration is calculated by number of levels:

$$P_{level} = 2(Q+1)^V - 1. \tag{1}$$

BDCLCMLI proposed the quantity of switches are given by Eq. (2):

$$R_{switch} = 2V + 4Q + P, \tag{2}$$

where P_{level} is the number of levels, R_{Switch} gives the quantity details of power switches used in BBCDCLMLI, Q – denotes the hybrid topology inverter, V – denotes the required amount of DC power and T – denotes the quality of DC-DC Cuk units.

2.2. Modes of operation

2.2.1. Approach denotes the BBC DC-link topology

For obtaining thirty-one-stage Alternating Current output using dual unbalanced power units, Designed structure will operate in four approaches.

• Operation modes A and B: In the operation modes 1 and 2, the source voltage SU_{dc1} is boosted to O_{obb1} by activating the BBC switch S_a and the DC-link switches are S_6 and S_7. The corresponding circuits for these modes are shown in Fig. 5(a) and (b).

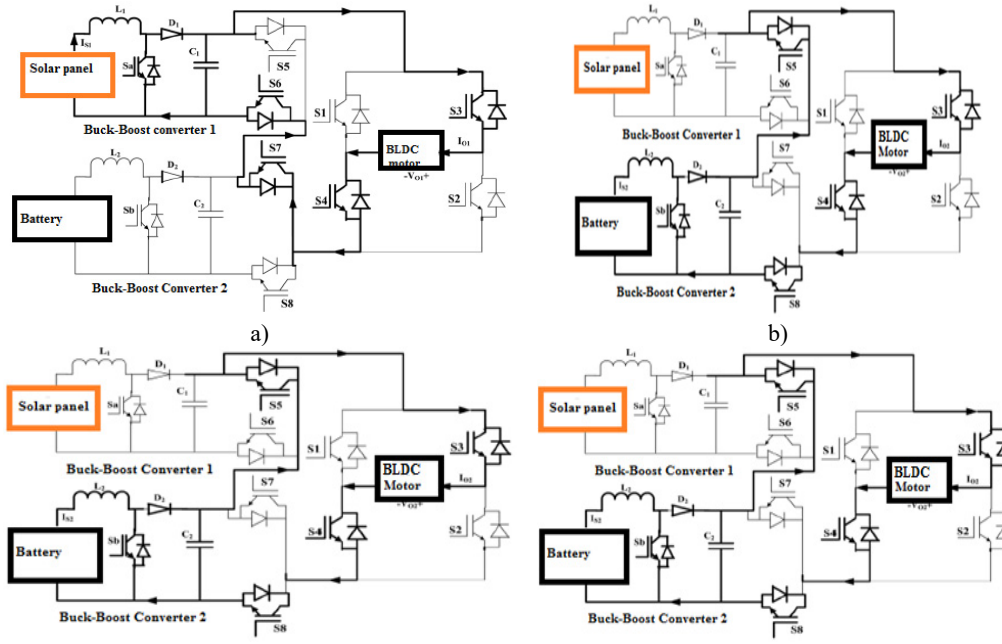


Fig. 5. Proposed model of operation modes: a) approach A, b) approach B, c) approach C, d) approach D

When $T = T_{ON1}$, the BBC converter device S_a energized correspondingly inductor current linearly increases towards I_1-I_2.

Inductor L_1 voltage are given as:

$$SU_{dc1} = L_1 \frac{I_2 - I_1}{T_{on1}}. \tag{3}$$

Energy to the inductor L_1 using source SU_{dc1} are obtained by:

$$ei1 = SU_{dc1} I_{sw1} T_{ON1}, \tag{4}$$

hence $T = T_{OFF1}$, BBC S_a switch energizes, inductor L_1 current decreases linearly at I_2-I_1.

Output voltage of converter 1 obtained using Eq. (5):

$$O_{obb1} = SU_{dc1} + L1_{T_{off1}}. \tag{5}$$

Inductor L_1 releases the energy which is fed to DCLM are obtained by Eq. (6):

$$el_{ol} = (O_{ob1} - SU_{dc1}) I_{S_{1OFF1}}. \tag{6}$$

Average output voltage of DC-DC converter 1 with lossless are obtained by Eq. (7):

$$O_{obb1} = \frac{SU_{dc1}}{1 - K_1}. \tag{7}$$

Voltage variation across the capacitor C_1 can be expressed by Eq. (8):

$$DeltaC_1 = OI_1 \frac{[V_{OBB1} - L_1(I_2 - I_1)]}{F * C * O_{BB1}}, \tag{8}$$

where B_{dc2} is the DC input voltage 1, I_{s2} determines the current source 1, K1 denotes the duty ratio of DC-DC converter 1, V_{obb1} is the load output of buck boost converter 1.

• Operation modes C and D: In operation modes E and H, the input voltages SU_{dc1} and B_{dc2} are Stepped up to V_{obb1} and V_{obb2} by energizing the buck boost converter devices S_a and S_b. Switches S_6 and S_8 conducts.

When $T = T_{ON3}$, the buck boost converter switches S_a and S_b are energized, and the current through the inductors L_1 and L_2 increases linearly from I_1 to I_2 and from I_3 to I_4, respectively.

At $t = T_{OFF3}$, enhanced converter S_a and S_b switches are de-energized accordingly inductor current L_1 and L_2 deenergizes linearly from I_2-I_1 and from I_4-I_3, correspondingly:

$$B_{dc2} = L_2 \frac{I_4 - I_3}{T_{ON2}}. \tag{9}$$

Inductor L_2 gets the energy fed via source obtained using Eq. (10):

$$e_{i2} = B_{dc2} I_{s2} T_{ON2}, \tag{10}$$

hence $T = T_{OFF2}$, the BBC device S_b are deenergized, inductor L_2 current decreases linearly from I_4-I_3.

Hence the voltage across converter 2 given by using Eq. (11):

$$V_{obb2} = BV_{dc2} + L_{2T_{OFF2}}. \tag{11}$$

Inductor L_2 releases energy which is fed DCLM are obtained by Eq. (12):

$$e_{o2} = (V_{ob2} - V_{dc2}) I_{s2} T_{OFF2}. \tag{12}$$

Average output voltage of DC-DC converter 2 with lossless are obtained by Eq. (13):

$$O_{oBb2} = \frac{B_{dc2}}{1 - K_2}. \tag{13}$$

A model of single-phase BBCDCLCMLI-based motor for 195V (V_{max}) output voltage was designed. Fig. 6(a), (b) represents Carrier signals, PWM pulses using n-levels. Experimental hardware has rectifier units, buck boost converter units, controller units, driver units, DC-link and H-bridge inverter units. Capacitive filter of 1000 μF, bridge rectifier (MICBR1010) are used for designing rectifier unit. The input converter units and battery banks are fed from the outputs of rectifier units. The buck boost converter (1 and 2) are fabricated using IRF840 controlled power devices (MOSFET) switches and passive components ($L_1 = L_2 = 2$ mH and $C_1 = C_2 = 100$ μF). MOSFET driver circuit gets control signals from dspic units. The features of dspic are used to achieve successful control of the proposed system. The proposed experimental diagram BBCDCLCMLI system is shown in Fig. 5(c). Table 1 shows the power-controlled devices turning states at various levels.

Capacitor C_2 voltage change is obtained by Eq. (14):

$$DeltaC_2 = OI_2 \frac{[V_{OBB2} - L_2(I_4 - I_3)]}{F * C * O_{BB2}}, \tag{14}$$

where B_{dc2} is the DC input voltage 2, I_{s2} determines the current source 2, K_2 denotes the duty

ratio of DC-DC converter 2, V_{obb2} is the load output of buck boost converter 2.

• Operation modes E and H: In operation modes E and H, the input voltages SU_{dc1} and B_{dc2} are Stepped up to V_{obb1} and V_{obb2} by energizing the buck boost converter devices S_a and S_b. Switches S_6 and S_8 conducts.

Table 1. Power controlled devices turning state of BBCDCLMLI

Potential rating, Volts	States level	Switch turning levels								
		s_a	s_b	s_1	s_2	s_3	s_4	s_5	s_6	s_7
30	1	0	1	1	1	0	0	0	1	1
35	2	1	0	1	1	0	0	1	0	0
40	3	0	1	1	1	0	0	0	1	0
45	4	1	1	0	0	0	0	0	0	0
50	5	0	1	0	0	1	1	0	1	1
55	6	1	0	0	0	1	1	1	0	0
60	7	0	0	0	0	1	1	0	1	0
65	8	0	0	0	0	1	1	0	1	0
70	9	0	1	1	1	0	0	0	1	1
75	10	1	0	1	1	0	0	1	0	0
80	11	0	1	1	1	0	0	0	1	0
85	12	1	1	0	0	0	0	0	0	0
90	13	0	1	0	0	1	1	0	1	1
95	14	1	0	0	0	1	1	1	0	0
100	15	0	0	0	0	1	1	0	1	0
105	16	0	0	0	0	1	1	0	1	0
110	17	0	1	1	1	0	0	0	1	1
115	18	1	0	1	1	0	0	1	0	0
120	19	0	1	1	1	0	0	0	1	0
125	20	1	1	0	0	0	0	0	0	0
130	21	0	1	0	0	1	1	0	1	1
135	22	1	0	0	0	1	1	1	0	0
140	23	0	0	0	0	1	1	0	1	0
145	–	0	0	0	0	1	1	0	1	0
140	24	0	1	1	1	0	0	0	1	1
155	25	1	0	1	1	0	0	1	0	0
160	26	0	1	1	1	0	0	0	1	0
165	27	1	1	0	0	0	0	0	0	0
170	28	0	1	0	0	1	1	0	1	1
175	29	1	0	0	0	1	1	1	0	0
180	30	0	0	0	0	1	1	0	1	0
195	31	0	0	0	0	1	1	0	1	0

When $T = T_{ON3}$, the buck boost converter switches S_a and S_b are energized, and the current through the inductors L_1 and L_2 increases linearly from I_1 to I_2 and from I_3 to I_4, respectively.

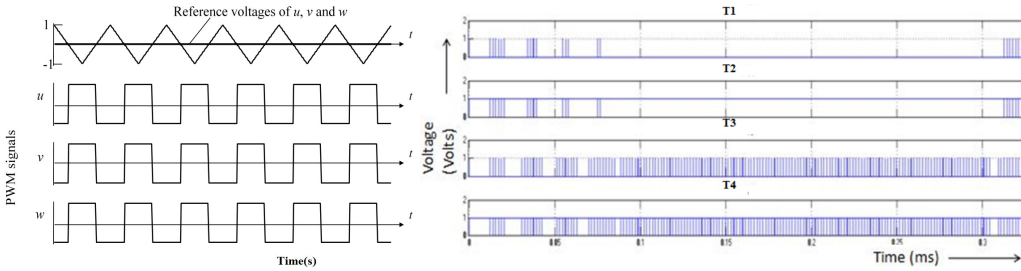
At this instant, the energy input to the inductor L_1 from the source SU_{dc1} and the energy input to the inductor L_2 from the source B_{dc2} are expressed using Eq. (15):

$$e_{i3} = (SU_{dc1} + B_{dc2})(I_{s_1} + I_{s_2})T_{ON3}. \tag{15}$$

At $t = T_{OFF3}$, enhanced converter S_a and S_b switches are de-energized accordingly inductor current L_1 and L_2 deenergizes linearly from I_2-I_1 and from I_4-I_3, correspondingly.

Hence situation, released inductors energy L_1 and L_2 of DCLM is determined as:

$$e_{03} = \left(V_{obb_1} - SU_{dc_1}\right)I_{s1} + \left(V_{obb_2} - B_{dc_2}\right)IS_2T_{off3}. \tag{16}$$



a) b)

Fig. 6. a) Carrier signal, b) PWM pulses for proposed system

2.2.2. Hybrid topology inverter bridge configuration operation

The cascaded multilevel inverter is made out of various single-stage H-bridge inverters and is ordered into symmetric and asymmetric groups in light of the size of dc voltage sources. In the symmetric kinds, the sizes of the dc voltage sources of all H-spans are equivalent while in the asymmetric sorts, the estimations of the dc voltage wellsprings of all H-spans are extraordinary. At present, a few topologies with different control strategies have been introduced for cascaded multilevel inverters. This research considered this H bridge concept and implemented in this system. The above topology inverter unit operates in dual operation. Alternating current at positive voltage are obtained with the use of Eqs. (17)-(19):

$$SU_{01} = v_{obb1}, \tag{17}$$
$$B_{02} = vobb_2, \tag{18}$$
$$v_o = SU_{01} + B_{02} = v_{obb1} + v_{obb2}. \tag{19}$$

At approach (b), the alternating current output voltage at negative cycle are synthesized and energized by Hybrid power devices S_3 and S_4 are given in Figs. 5(b) and (d).

Alternating current at negative voltage are obtained by:

$$SU_{01} = -V_{ob1}, \tag{20}$$
$$B_{02} = -V_{0b2}, \tag{21}$$
$$TV_0 = [V_{01} + V_{02}] = -[V_{ob1} + V_{ob2}]. \tag{22}$$

2.2.3. Buck boost converter conduction losses

MOSFET switching losses are calculated using the accurate voltage drop with series linear resistor $R_D = 0.07$. It determines the terminal gate by terminal source voltage and junction temperature. The losses in the MOSFET switch are given in Eq. (23):

$$P_{cond} - S_2 = I_{S_{1,2}}^2 X R_{DS_{on}}, \quad I_{S_{1,2}}^2 = D_2 X \left[I_{OS_{1,2}}^2 + \frac{\Delta I_{OS_{1,2}}^2}{12} \right], \tag{23}$$

where I_{s2} indicates the current flowing through the switch S_2, S_2 stands for the "ON" time of switch and delta I^2 stands for the average ripple current of switch. Switching ampere determined as I_{OS_2} is derived from Eq. (23):

Harmonics current $\Delta I_{OS_{1,2}}$ are given as in Eq. (24):

$$\Delta I_{OS_{1,2}} = \frac{I_{OS_{1,2-max}} - I_{OS_{1,2-min}}}{2} = \frac{8.53 - 6.6}{2} = 0.965, \tag{24}$$

where $I_{OS_{1,2}-max}$ and $I_{OS_{1,2}-min}$ gives high and low magnitudes of power-controlled device current S_1-S_8 as illustrated in Fig. 7. From Fig. 6, $D_2 = 0.22$, $I_{OS_2} = 7.565$ and $\Delta I_{OS_{1,2}} = 0.965$, which are substituted in Eq. (24), sum amperes and losses are derived from MOSFET switches as resolved in Eq. (25):

$$I_{S_{1,2}}^2 = 12.58 \text{ A}, \quad P_{cond} - S_{1,2} = 12.58X0.069 = 0.90 \text{ W}. \tag{25}$$

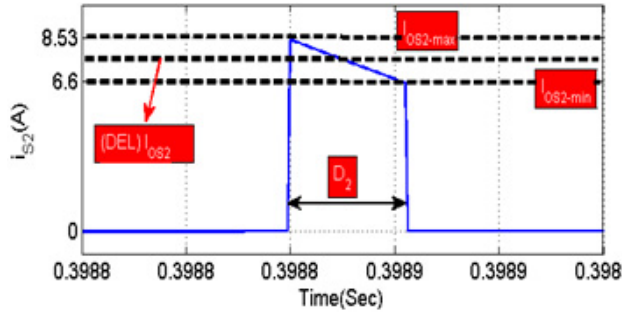


Fig. 7. MOSFET switches conduction waveform at open-loop condition

2.2.3.1. Switching conduction losses $S_{1,2}$ during starting

Buck boost Cuk converter diode D losses.

Converters diode D losses due to forward voltage $V_{F1} = 0.8$ V are expressed by Eq. (26):

$$PL_{D1} = I_{D1}XV_{F1}, \quad I_D = D_dX\left[I_{OD}^2 + \frac{\Delta I_{OD}^2}{12}\right], \tag{26}$$

where I_{D1} is ampere via diode, D represents "ON" time of diode, hence the harmonic amps are obtained from Eq. (27):

$$\Delta I_{OD1} = \frac{I_{OD1-max} - I_{OD1-min}}{2} = \frac{6.5 - 0}{2} = 3.25, \tag{27}$$

where $I_{OD1-max}$, $I_{OD1-min}$ represents the high and low magnitudes of diode, which is shown in Fig. 8. Fig. 8 shows $D_{d1} = 0.15$, $I_{OD1} = 0$ and $\Delta I_{OD1} = 3.25$ and total torque ripple voltage across each components. The values are substituted in Eq. (27), the total current conduction and the power loss of diode, as resolved in Eq. (28):

$$I_{D1} = 0.132 \text{ A}, \quad PL_{D1} = 0.132X0.8 = 0.1 \text{ W}. \tag{28}$$

2.2.3.2. Converters inductor losses L_1 and L_2

The open-loop waveforms of converter inductor are shown in Fig. 8. Meanwhile, inductor losses L_1 and L_2 have two factors. First factor is wire loss or core loss. It is given by Eq. (29) for a wire:

$$PL_{L1} = I_{L1}^2XR_{dcL1}, \quad I_{L1}^2 = D_{L1}X\left[I_{oL1}^2 + \frac{\Delta I_{oL1}^2}{12}\right]. \tag{29}$$

Therefore, the mean harmonic current is given in Eq. (30):

$$\Delta I_{OL1} = \frac{I_{OL1-max} - I_{OL1-min}}{2} = \frac{10.5 - 0}{2} = 5.25. \quad (30)$$

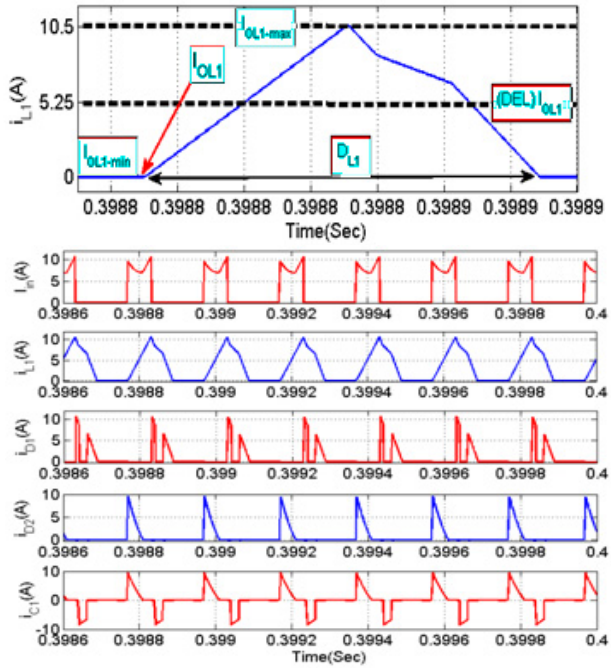


Fig. 8. Converter: a) diode losses, b) ripple voltages across components [24]

3. Results and discussions

3.1. Simulation performance evaluation

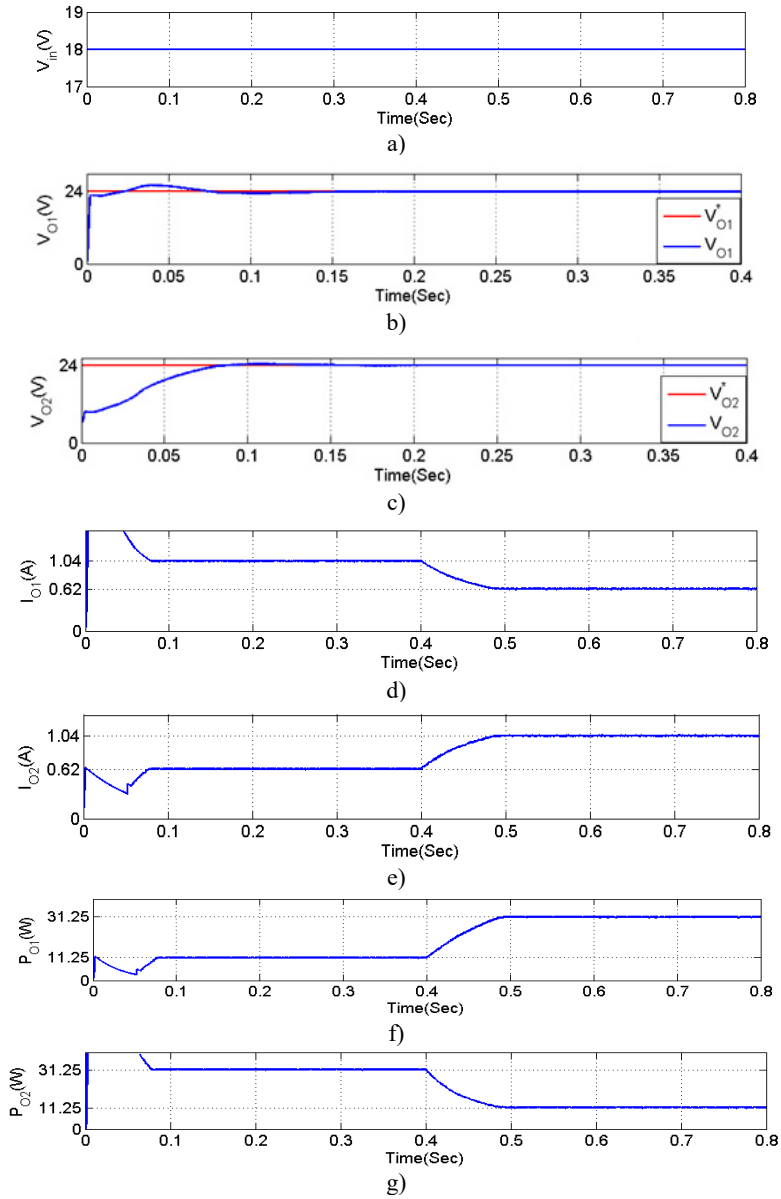
The proposed control topology is tried with a perfect three-stage connection with a two-phase BBC power supply and a permanent magnet synchronous motor load. Simulation Specifications are shown in Table 2.

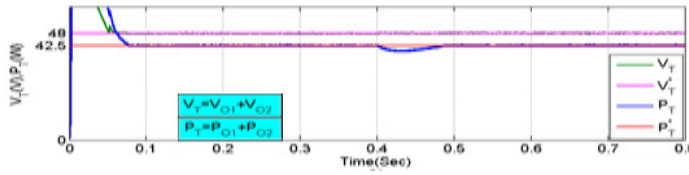
Table 2. Simulation specifications for converter

S. No	Objects	Values
1	Maximum PV module voltage	24 V
2	Maximum PV module current	1.04 A
3	Maximum PV module power	74 W
4	TPC output voltage	48 V
5	TPC output power	40 W
6	Rated BLDC motor power (Torque = 0.125 Nm, Speed = 2000 Rpm, DC link voltage = 24 V, number of poles = 8)	39 W
7	Nominal power of battery (Nominal voltage = 12 V, Nominal current = 7 A/h)	84 W/h

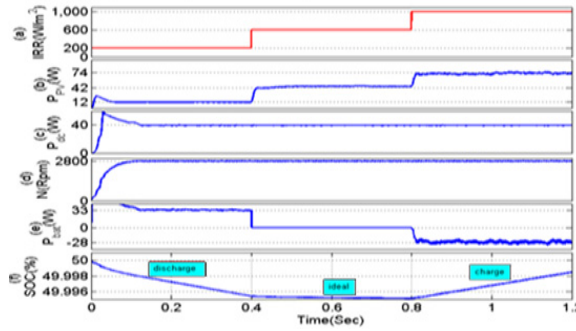
To verify the asymmetrical performance of converters, an input DC voltage source is considered to be $V_{in} = 18$ V as shown in Fig. 9. Further, load resistances $R_1 = R_2 = 28.8$ Ω are considered for a symmetrical condition. The output voltages of the MOBB converter are desired to be regulated on $V_{O1} = 30$ V and $V_{O2} = 18$ V from 0 to 0.4 Sec. At a particular time, i.e. from 0.4 Sec to 0.8 Sec, the MOBB converter output voltages are desired to be regulated on $V_{O1} = 18$ V and $V_{O2} = 30$ V respectively. In Figs. 9(b) and (c), output voltages V_{O1} and V_{O2} are shown. As seen from this figure, the output voltages are tracked by the reference values V_{O1}^* and V_{O2}^* with a

minimum steady state error. It is obvious that the output voltages are regulated very well. Similarly, the currents I_{O1} and I_{O2} are drawn from load resistances R_1 and R_2 as shown in Fig. 9(d) and (e). At this time, load resistances $R_1 = 31.25$ W and $R_2 = 11.25$ W consume power from the input supply till 0.4 sec, consequently after 0.4 sec load, resistances consume power from the input supply 11.15 W and 31.25 W respectively. Therefore powers P_{O1} and P_{O2} are drawn under asymmetrical output voltage condition as shown in Fig. 9(f) and (g). In Fig. 9(h), the total output voltage $V_T = V_{O1} + V_{O2}$ and total output power $P_T = P_{O1} + P_{O2}$ are represented. As seen from this figure, voltage and power are tracked by the reference values $V_T^* = 48$ V and $P_T^* = 42.5$ W. It is obvious that the output voltage and power are regulated smoothly. Fig. 9(i) and (j) shows battery, motor outputs. The converter works in three conditions by using battery BCD, PVD, BDD.

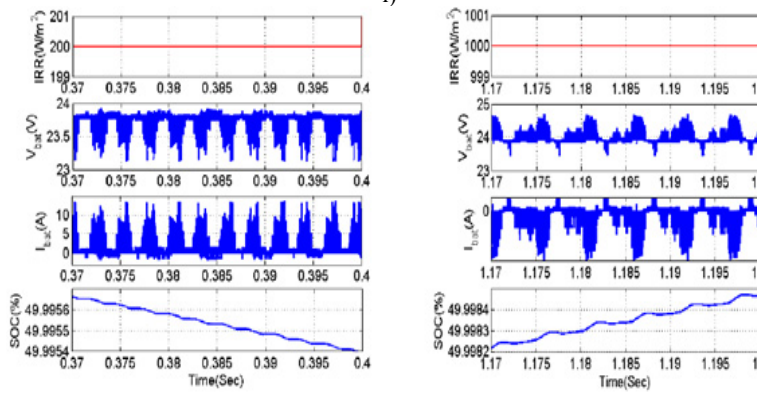




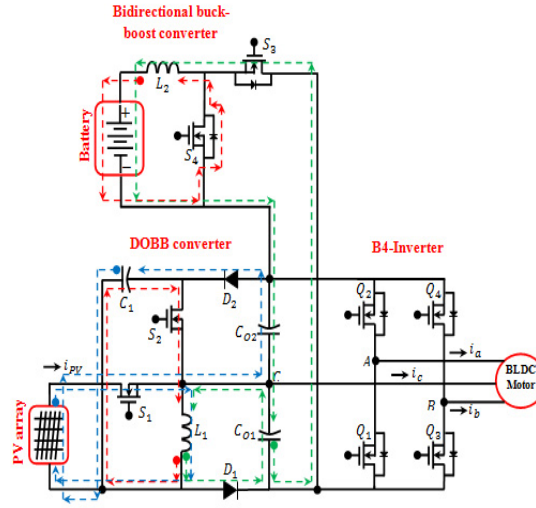
h)



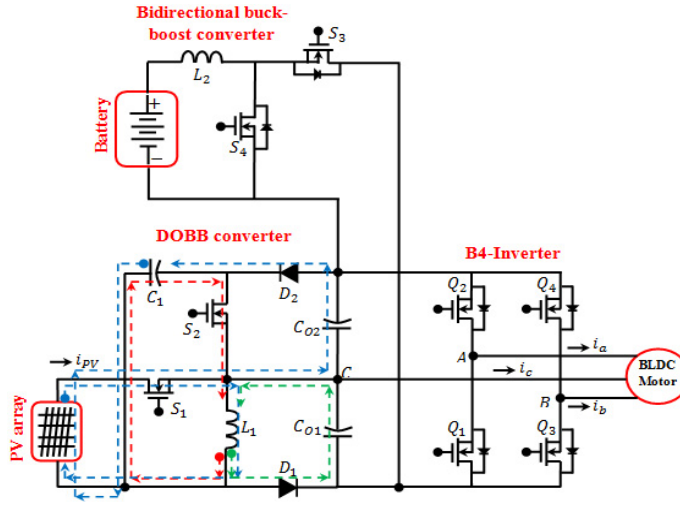
i)



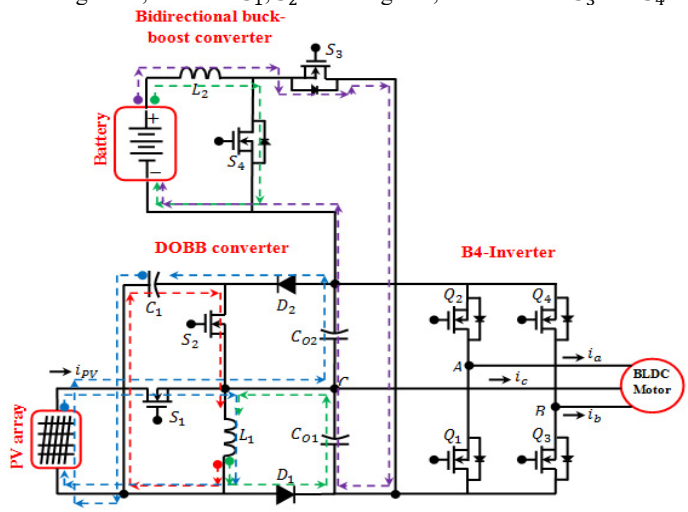
j)



k) In this mode, PV both supplies load and delivers power to battery. This condition occurs when PV power is maximum as compared with the load power, therefore the battery must to be charged. In BCD, switches S_1, S_2, S_3 are active and switch S_4 is entirely OFF



l) With the above approach, PV only supplies loads. This situation acts when PV power is equal to motor power. During PVD, switches S_1, S_2 are energized, and switches S_3 and S_4 are OFF



m) In the above approach, dual sources PV and battery are energized for delivering the load. In BDD, switch S_3 is OFF, and switch S_1, S_2, S_4 are ON

Fig. 9. a)-h) Converter asymmetrical output, battery, i), j) motor parameters outputs, k) BCD, l) PVD, m) BDD [24]

The converter outputs are fed to multilevel inverter switches. The recreation parameters are set as follows: supply frequency = 50 Hz, input voltage = 480 V, input current = 27 A, exchanging frequency = 2 kHz, resistance = 20 Ω, inductance =310 mH for 31 level inverter; using the MATLAB platform, the output voltage are synthesized. Multilevel inverters with 31-levels output voltage synthesis are shown in Fig. 10.

Figs. 10, 11 and 12 display steady state conditions of the simulated output voltage, current waveforms and the harmonic profile of the output voltage. To get an equation for THD, please note that the average power of the cosine at a single harmonic is given by:

$$P_k = 2|C_k|^2, \tag{31}$$

where $k = 1$ represents the fundamental and $k \geq 2$ are the harmonics. Also note that the total average power in the signal is given by the sum of the average powers at each harmonic:

$$P = |C_0|^2 + \sum_{k=1}^{\infty} P_k = |C_0|^2 + \sum_{K=1}^{\infty} 2|C_k|^2. \tag{32}$$

As such the THD can be calculated by finding the total power in all harmonics divided by the power in the fundamental:

$$THD = \frac{P_2 + P_3 + P_4 + \cdots}{P_1} = \frac{2|C_2|^2 + 2|C_3|^2 + 2|C_4|^2 + \cdots}{2|C_1|^2}. \tag{33}$$

In reality, there is no way to measure the infinite harmonic, so the THD measurement is usually truncated to a certain harmonic. Also note that the Fourier coefficients are required for this measurement but that the spectrum analyzer provides values in dBmV:

$$P_{dBmv} = 10\log_{10}\left(\frac{2|C_k|^2}{(0.001)^2}\right). \tag{34}$$

Because the THD is a ratio of powers, it is unit-less and is expressed as a percentage. It can also be expressed in dB as:

$$THD = 10\log_{10}\left(\frac{P_2 + P_3 + P_4 + \cdots}{P_1}\right). \tag{35}$$

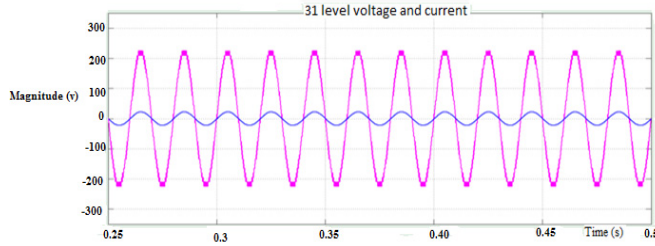


Fig. 10. Multilevel inverter with 31-levels output voltage synthesis

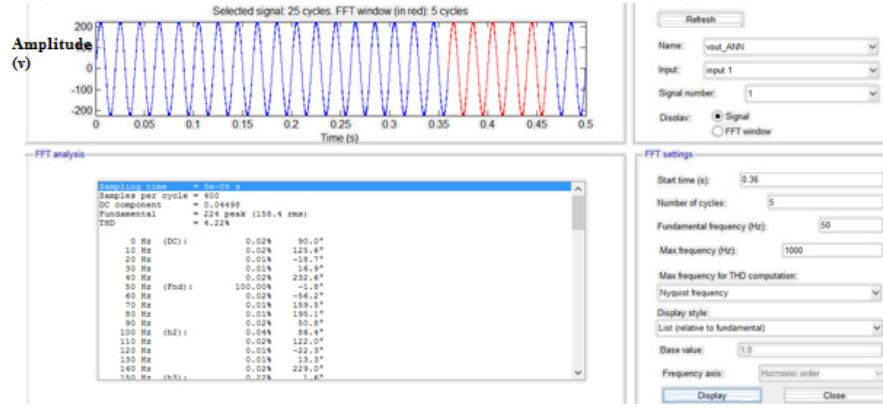


Fig. 11. THD for 31 level with Developed H bridge converter module

The study and analysis of the diode clamped 31-level inverter, flying capacitor-clamped 31-level inverter, cascaded 31-level inverter as well as the proposed bridged-insert cascaded 31-level inverter were carried out using MATLAB/ Simulink Tool. The voltage output obtained across the load or in other words, at the pole was analyzed and compared. Not only that, the FFT (Fast Fourier Transform) analysis was also done in order to analyze the harmonic distortion

present in the output. On comparison of the results obtained, it is evident that the proposed bridged-insert cascaded MLI is much more superior to the other discussed topologies when comparing the total harmonic distortion (THD) as well as the area usage. The various levels are analyzed from 5-level, nine level twenty-five level and thirty-one level.

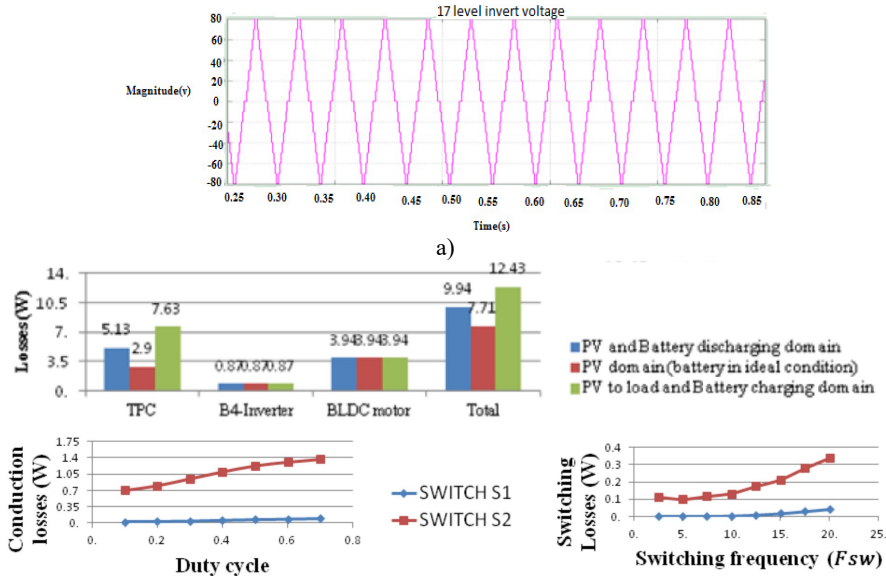
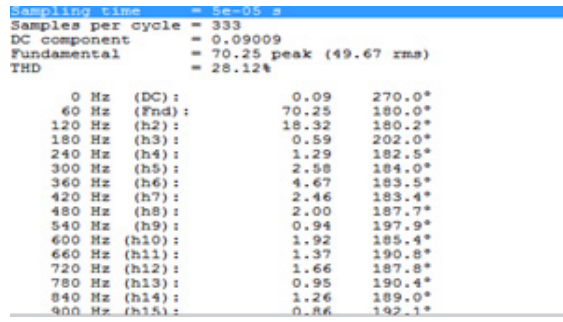


Fig. 12. a) Output voltage for 17-level MLI, b) losses, duty cycle



```
Sampling time       = 5e-05 s
Samples per cycle   = 333
DC component        = 0.09009
Fundamental         = 70.25 peak (49.67 rms)
THD                 = 28.12%

   0 Hz   (DC):          0.09     270.0°
  60 Hz   (Fnd):        70.25     180.0°
 120 Hz   (h2):         18.32     180.2°
 180 Hz   (h3):          0.59     202.0°
 240 Hz   (h4):          1.29     182.5°
 300 Hz   (h5):          2.58     184.0°
 360 Hz   (h6):          4.67     183.5°
 420 Hz   (h7):          2.46     183.4°
 480 Hz   (h8):          2.00     187.7°
 540 Hz   (h9):          0.94     197.9°
 600 Hz   (h10):         1.92     185.4°
 660 Hz   (h11):         1.37     190.8°
 720 Hz   (h12):         1.66     187.8°
 780 Hz   (h13):         0.95     190.4°
 840 Hz   (h14):         1.26     189.0°
 900 Hz   (h15):         0.86     192.1°
```

Fig. 13. Harmonic analysis of 17 level inverter with developed H-bridge converter

3.2. Diode clamped MLI

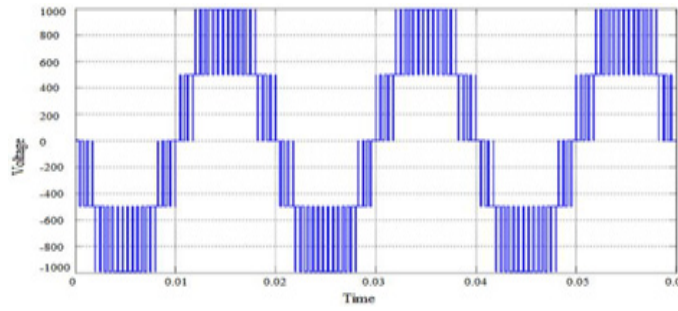


Fig. 14. The output voltage waveform of the 5-level diode-clamped MLI

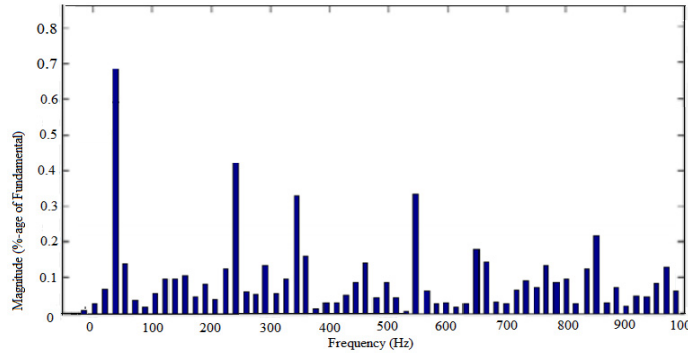


Fig. 15. The FFT of the 5-level diode-clamped MLI. Fundamental (50 Hz) = 38.7 Hz, THD = 21.97 %

3.3. Flying-capacitor clamped MLI

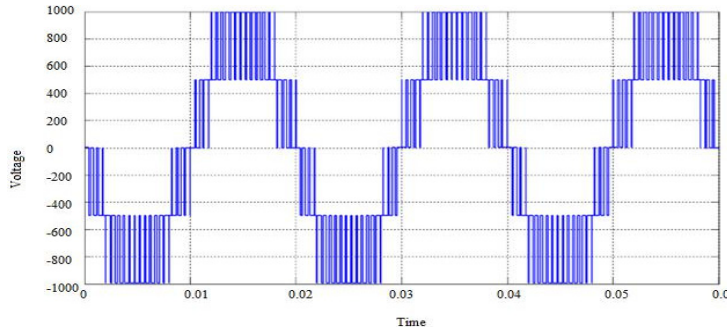


Fig. 16. The output voltage waveform of the 5-level flying capacitor clamped MLI

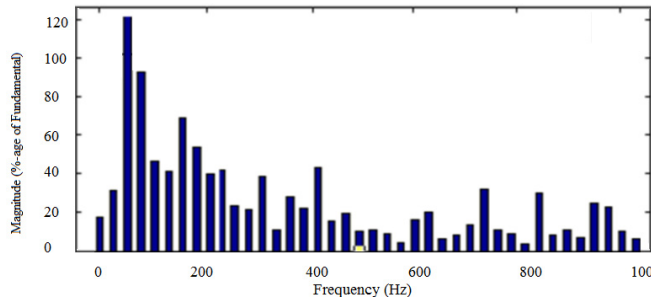


Fig. 17. The FFT of the 5-level flying capacitor clamped MLI. Fundamental (50 Hz) = 967.4 Hz, THD = 39.92 %

3.4. Conventional cascaded MLI

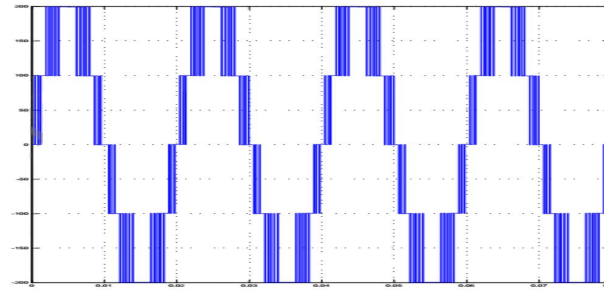


Fig. 18. The output voltage waveform of the 5-level cascaded MLI

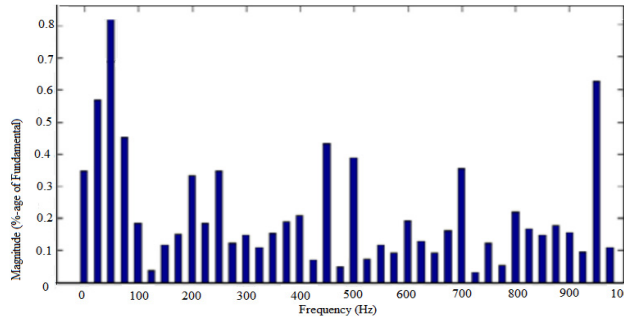


Fig. 19. The FFT of the 5-level cascaded MLI. Fundamental (50 Hz) =278.6 Hz, THD = 20.93 %

3.5. Novel bridged-insert cascaded MLI

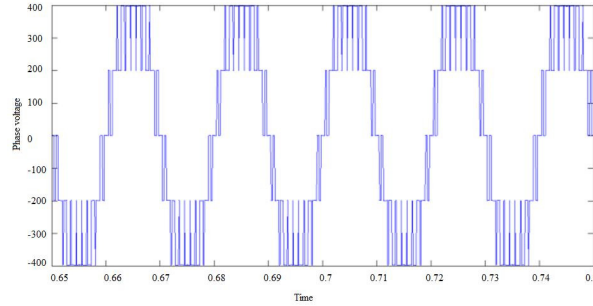


Fig. 20. The output voltage waveform of the 5-level bridged-insert cascaded MLI

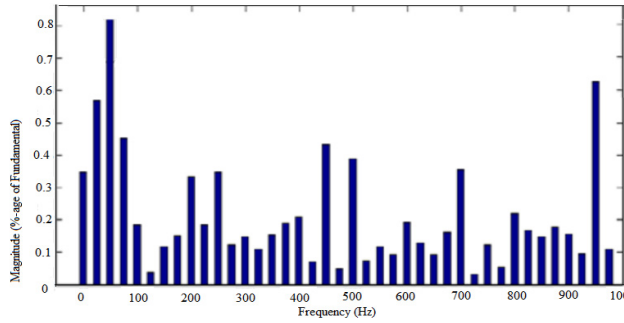


Fig. 21. The FFT of the 31-level bridged-insert cascaded MLI. Fundamental (50 Hz) = 120 Hz, THD = 18.93 %

3.6. Analysis and comparison

The results from section V have been consolidated in this section using bar-chart. Figs. 22, 23 show the comparison of the proposed bridged-insert cascaded MLI with diode-clamped, flying capacitor clamped and conventional cascaded MLI topologies in terms of the fundamental frequency, area coverage and THD as given in Table 3.

Table 3. Result summary

Type	Fundamental in Hz	THD in %-age	Area (number of transistors)
Diode-clamped	38.7	21.97	8
Flying-capacitor clamped	967.4	39.92	8
Conventional cascaded	278.6	20.93	8
Proposed	120	18.78	4

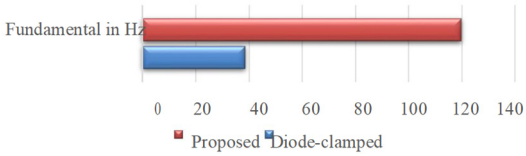


Fig. 22. Fundamental frequency comparison: diode-clamped MLI vs proposed

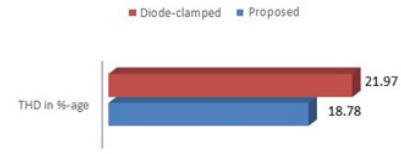
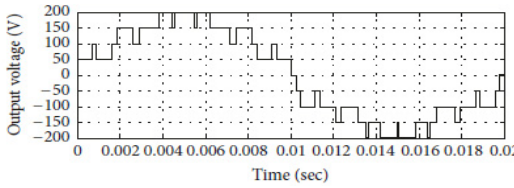


Fig. 23. THD comparison: diode-clamped MLI vs proposed

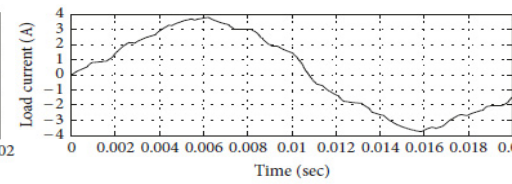
The Table 4 shows the various level comparisons.

Table 4. THD comparison of diode clamped and developed H-Bridge based 17 and 31 level MLI topology

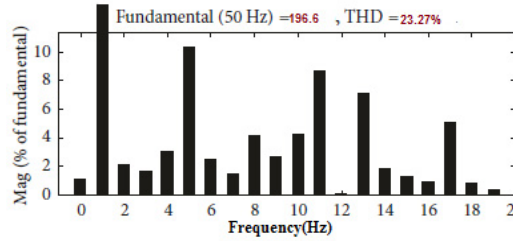
Parameter	Proposed	
	Diode clamped	Developed H bridge
THD for level 31 (%)	12.5	2.17
THD for level 9 (%)	46.11	4.77
THD for level 17 (%)	32.11	4.39
THD for level 24 (%)	22.09	4.30



a) Output voltage

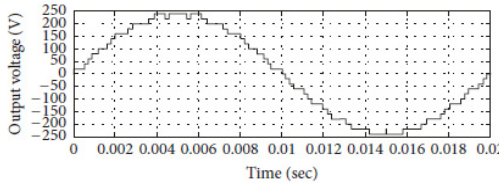


b) Load current

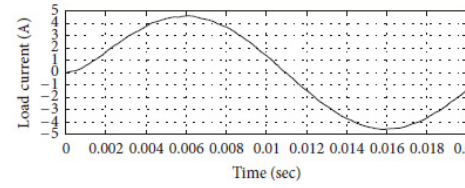


c) Harmonic contents of output voltage

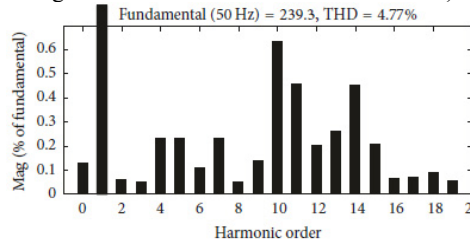
Fig. 24. Simulation result for nine-level cascaded circuit of multilevel inverter



a) Output voltage

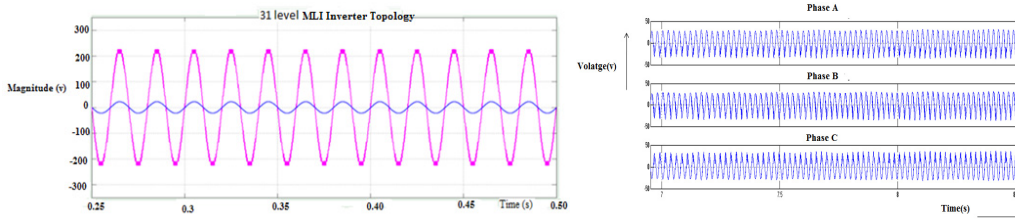


b) Load current

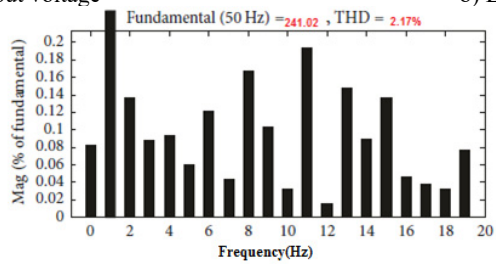


c) Harmonic contents of output voltage

Fig. 25. Simulation result for twenty five-level cascaded circuit of multilevel inverter



a) Output voltage b) Load current



c) Harmonic contents of output voltage

Fig. 26. Simulation result for thirty one-level cascaded circuit of multilevel inverter

3.7. Experimental evaluation

The converter outputs are fed to multilevel inverter switches. The recreation parameters are set as follows: supply frequency = 50 Hz, input voltage = 480 V, input current = 27 A, exchanging frequency = 2 kHz, resistance = 20 Ω, inductance =310 mH for 31 level inverter. Table 5 indicates motor parameters.

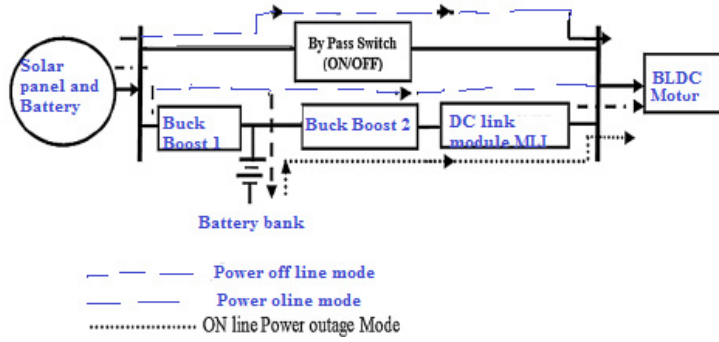


Fig. 27. Experimental circuit diagram of BBCDCLMLI

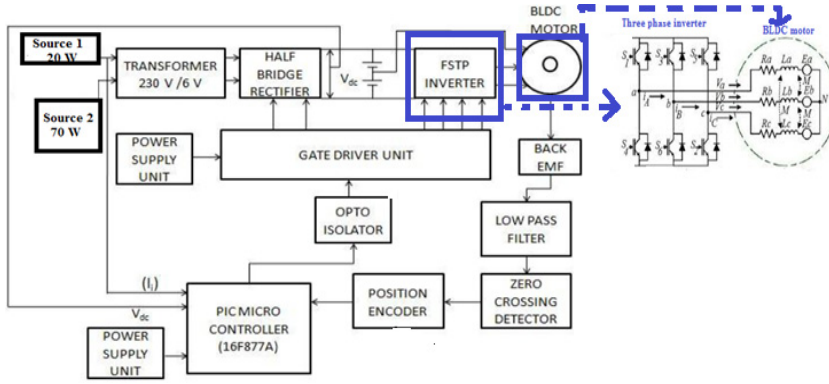


Fig. 28. Realization of hardware circuit diagram of BBCDCLMLI

The experimental circuit diagram and realization of hardware model are shown in Figs. 27 and 28. The corresponding effective results are carried as shown in Fig. 29. Prototype hardware circuit diagrams of BBCDCLMLI are shown in Fig. 30. Comparisons were carried out with various level inverters and proved with reduced torque ripple and vibrations, and noise was reduced with the proposed system.

Table 5. Motor parameters specifications

S.NO	Name of the equipment	Range
1	Battery	12 V/4.7 AH
2	Step down transformer	230 V/12 V
3	Step down transformer	230 V/5 V
4	MOSFET	IRFZ24N 17 A, 55 V, 0.07 ohm, N-CHANNEL, Si, POWER, MOSFET, 220 AB
5	BLDC motor	220 V, 100 A, 60 rpm

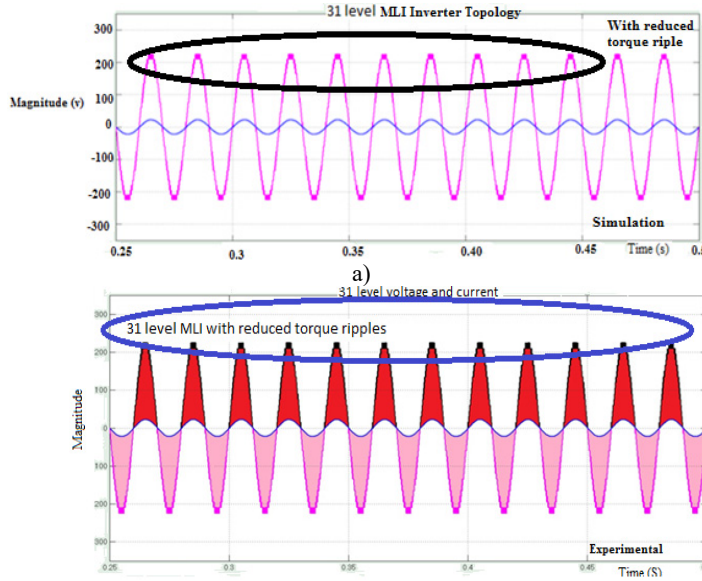


Fig. 29. Thirty-one-level MLI: a) simulation output, b) experimental output

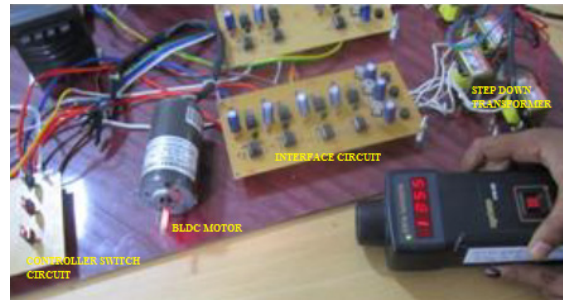


Fig. 30. Prototype hardware circuit diagram of BBCDCLMLI sensing speed

3.7.1. Reduction of mechanical vibration on motor and comparative analysis of total harmonic distortion

The major drawbacks of BLDC motor consist in torque ripple that causes mechanical vibrations and acoustic noise. In industry engineering of electric hybrid vehicles, the torque ripple

could result in mechanical vibration and acoustic noise. Thus, it is undesirable for most of the applications. In this research the Total Harmonic Distortion in the voltage and current waveform, RMS level of vibration, and noise has been examined, and their comparison is shown in table. The RMS level of the vibration is calculated using the Matlab software. The hardware prototype model was developed for BBCDCCLMI, torque ripples are calculated using a vibration sensor, and vibrations are calculated as shown in Fig. 31. This proves that the proposed BBCDCMMLI method is able to suppress the torque ripple and mechanical vibration, and its prototypes are shown in Fig. 32. Table 6 shows the comparison of various parameters for the measurement of vibration proposed is more efficient than the conventional.

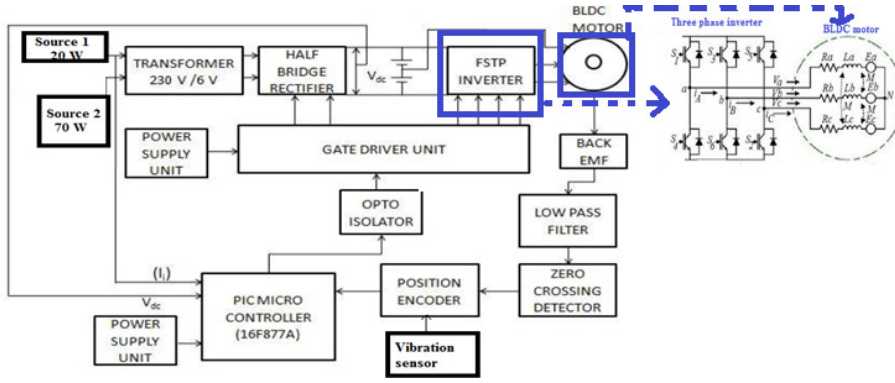


Fig. 31. Realization of hardware circuit diagram of BBCDCLMLI for sensing vibration

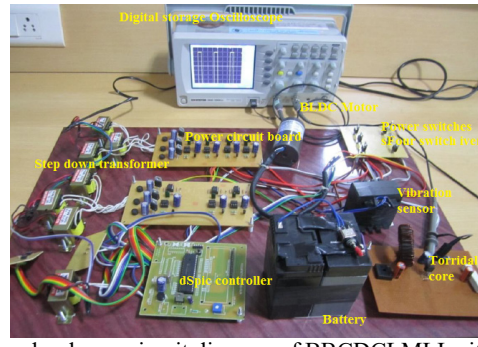


Fig. 32. Prototype hardware circuit diagram of BBCDCLMLI with vibration sensor

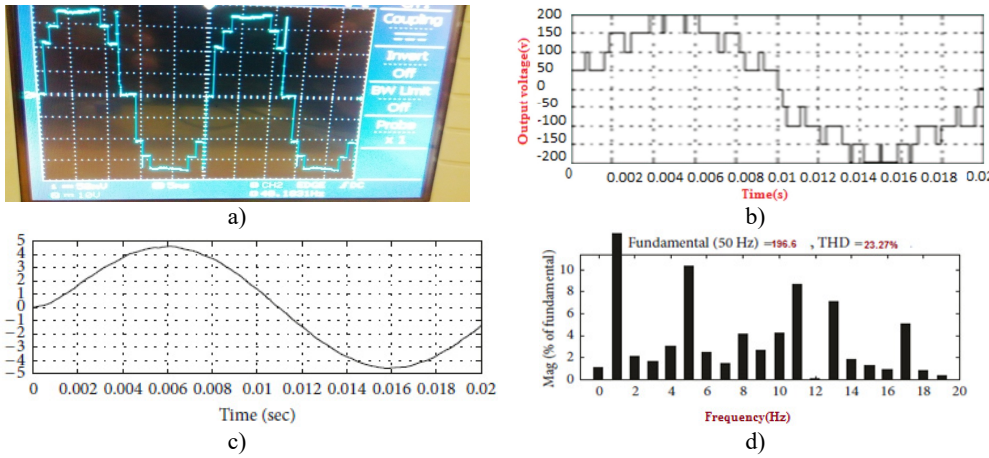


Fig. 33. Nine level MLI: a) experimental output, b) simulation output, c) load current, d) THD analysis

Fig. 33 shows the nine-level experimental output it have more harmonics compared with the 32 level based on the reduction of vibrations. Table 6 shows the Comparison of various parameters to measure vibration using THD analysis chart as shown in Fig. 34.

Table 6. Comparison of various parameters to measure vibration

Parameter	Diode clamped	Developed H bridge	Torque ripple	Current ripple
Proposed THD for level 31 (%)	12.5	4.22	0.6	0.7
THD for level 17 (%)	32.11	28.12	0.66	1.2
THD for level 27 (%)	20.5	21.12	0.71	1
THD for level 9 (%)	27	18	0.89	1.6

Table 7. Comparison of converter for MLI

Particulars	Converter presented by Zhu et al. (2015)	Proposed converter for MLI
Losses when converter operates in SD	4.21 W	6.42 W
Losses when converter operates in MBCD	1.69 W	2.86 W
Losses when converter operates in MBDD	2.1 W	3.52 W
Total losses when converter operates in all distribution domains	8 W	12.8 W
Average efficiency when converter operates in all distribution domains	93.81 %	90.47 %
Total number of components	11	12
Type of conversion	$V_T > V_{in}$ (Buck)	$0 > V_T > V_{in}$ (Buck-Boost)
Possibility of output voltage control	V_T	(V_{O1} or V_{O2}) $< V_T$
Driver circuit complexity	Complex	Simple

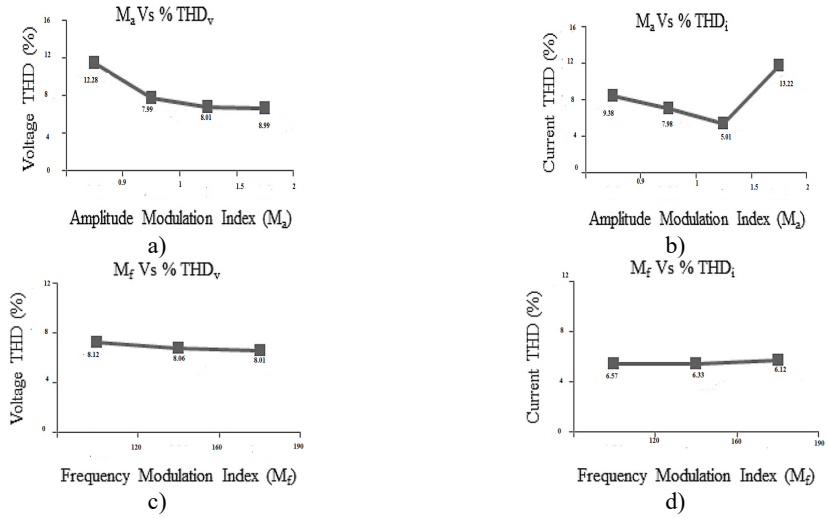


Fig. 34. THD analysis chart

4. Conclusions

The proposed Subsystem contains the hybrid quasi converters with two sources, namely wind and solar ones. Its source networks having boost abilities are used to step up the voltages from photovoltaic systems and from wind energy. In any case, the customary DC-DC systems have a few confinements to help the voltages, and there is discontinuity of input current and voltage and current burdens. To solve the above issues, adjusted and combinational source systems are fabricated to be utilized for distinguishable applications from customary systems with expanded

effectiveness and even cost effective. The level of the harmonics and its supply power were analyzed and reduced. It is designed with both 17-level and 31-level diodes clamped based on the converter unit. The H bridge topology was developed with MATLAB/Simulink. Finally, the operation of total subsystem is verified based on the harmonic reduction. From the experimental results, it is concluded that the proposed Subsystem with the developed H bridge converter has the least total harmonic distortion as 4.22 % and 28.12 % for 31-level and 17-level MLI topology respectively.

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