Analysis and design of a novel hybrid topology for power quality improvement using multilevel inverter fed induction motor by reducing vibration for textile wastewater treatment applications

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Abstract. The proposed research involves the design and implementation of a novel hybrid topology for power quality improvement using multilevel inverter fed induction motor by reducing vibration for Textile applications. Various modern applications have started to require higher power gadgets as of late. Staggered inverter is equipped for giving wanted substituting voltage level at output utilizing different low-level DC voltage as an input. In H-connect staggered inverter, the quantity of output level is characterized by the quantity of exchanged capacitor cells. A small amount of voltage can be utilized to produce a supported output voltage by exchanging the capacitor in parallel and in series. Staggered inverter produces less Total Harmonic Distortion (THD), less electromagnetic interference and less voltage inrush on switches. The proposed topology delivers a staircase waveform with higher number of output level utilizing less segments contrasted with a few existing exchanged capacitor multilevel inverter. The task manages cascaded H-connect staggered inverter that can be utilized for both single and three stage change. The structure is created with H-bridge inverter including DC-DC converter. A sine pulse width twist is decided on PWM pulses. The inverter essentially takes care of the issue of capacitor voltage adjusting as every capacitor is charged to the esteem equivalent to one of the information voltages at each cycle. Recreation is finished with the assistance of MATLAB Simulink programming and the exploratory outcomes for current and voltage at various THD esteems are appeared and the equivalent is done for equipment. The prototype structure is conceded and analysed for various parameters of proposed method, which results in reduced switches and proves more efficient than other conventional methods and in addition it is more proficient for pumping process in textile industry for wastewater treatment.

Keywords: DC-DC converter, induction motor, photovoltaic panel, multilevel inverter, vibration, ampere-hour unit.

1. Introduction

Industrial applications consist of two main areas, motor control and power supplies. The electric utility in industry faces deregulation and characteristic changes are frequently professed. Flexible AC Transmission Systems (FACTS), High-Voltage Direct Current (HVDC) and Custom Power Headway are based on power electronics, which include a fragment of the most encouraging explicit developments, to deal with the new operational difficulties, being revealed today. These degrees of advancement depend upon a superior point of confinement of essentialness electronic mechanical assembly so as to rapidly respond to structure events. So, the addition control trade confines and improves the idea of vitality passed on. In the recent years, the powerful applications are driving the world with the regard of their wide extending thought. Since, various topologies, systems and drive applications are evaluated and examined. Such converters

are sensible with high power gadgets dependent on their rating. Reference [1, 2] encircled the staggered power transformation topology with impartial point cinched topology. Ongoing days, the interest in gadgets was related with many quick charging gadgets which outer vitality sources require early examination on consonant and non-dynamic power remuneration [3]. This far reaching symphonious dirtying gadget both lessens the framework effectiveness, and impact affects lattice voltage mutilation levels [4, 5]. Thus, the expansion of flow prompts heat misfortunes and makes a few issues in touchy electrical gadgets. Some ongoing scientists are centered around power quality issues and current music. Power Quality is the best approach to successful movement of value thing and the action of an industry. The growing prominence on the general power system viability realized the use of gadgets, for example, high adequacy, adaptable speed motor drives and shunt capacitors for control factor solution for decline misfortunes achieving extending consonant dimensions on control structures. For different applications like farming and modern diverse topologies of intensity controlled gadgets are intended to insert with the sustainable assets. From this time forward Multilevel inverters (MLIs) are developing as a current logical thing of intensity controlled gadgets for high-control applications. The three noteworthy MLIs are Diode clamped MLI, Flying Capacitor MLI (FC MLI) and Cascaded Single Pulse Staggered Inverters MLI (CSPSI MLI) [6, 7]. CMLI makes the ventured AC voltage waveform with more DC sources with decreased symphonious material. CMLI goes about as a more interesting topology than the other two topology. Cascaded Conventional circuit with single pulse input is shown in Fig. 1.

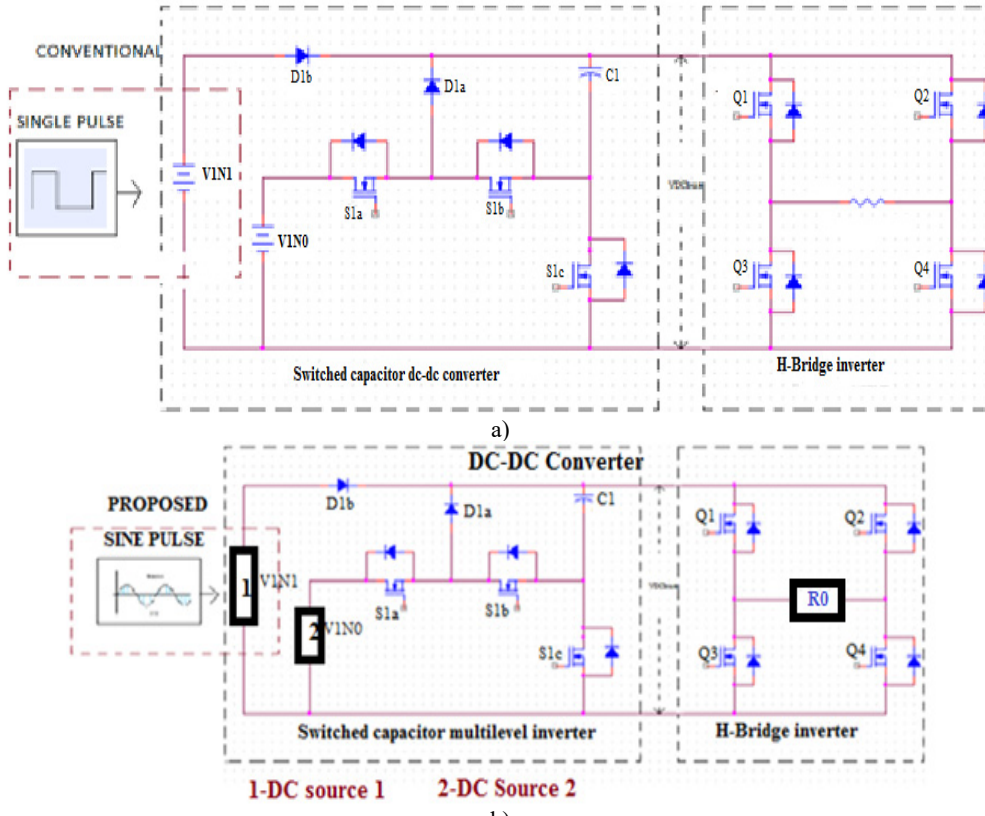


Fig. 1. a) Conventional schematic circuit diagram of single pulse CCSPMLI, b) proposed schematic circuit diagram of CCSPMLI with load R_0

The circuit is fed with the sine pulse and ramp signal for proposed method is shown in Fig. 2.

The proposed multilevel inverter is fed with induction motor (MLIFIM).

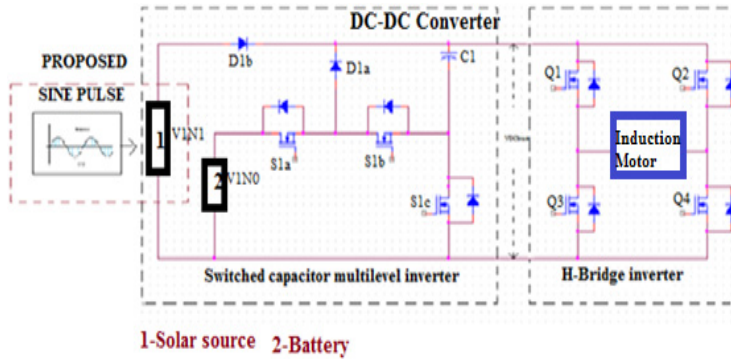


Fig. 2. Schematic circuit diagram with load of MLIFIM

For acquiring output ostensible in CCMLI, new topology staggered converter topology is proposed between the different info sources either thinking about transformer. The productivity and treatment of CCMLI and buck-help CMLI (BBMLIFIM) set ups are degraded as a result of a lot of prohibited power controlled switches and DC sources. The proposed cascaded DC link circuit diagram is shown in Fig. 3.

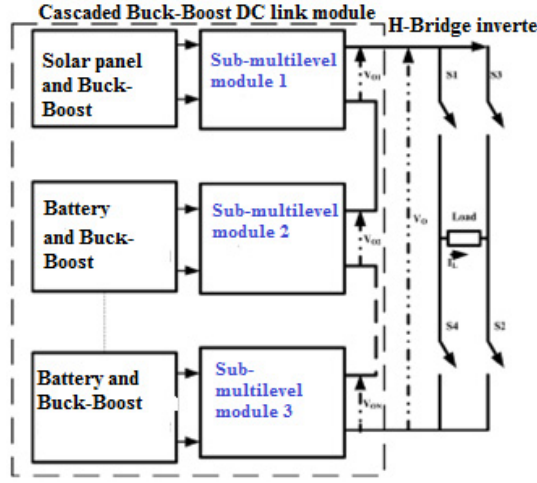


Fig. 3. Proposed structure of Buck-Boost cascaded DC-link multilevel inverter

In the interim topological adjustments are made in the current CCMLI [8-12]. From now on in proposed investigate, the buck-boost converter circuit is presented between information sources and DC-connect inverter to acquire ostensible output voltage. Such changes of topology results in the decrease of intensity controlled gadgets advertisement input sources. For this research, a single-stage seven-level and Buck Boost DC-interface CMLI fed induction motor (BBDCCMLIFIM) framework is intended for business applications. Schematic circuit of the proposed BBDCLCMLIFIM framework is appeared in Fig. 4.

To reduce the Total Harmonic Distortion (THD) occurred with the single pulse contribution as proposed [13-16], To overcome this disadvantages, changed sine wave and ramp wave is utilized as an elective strategy in the exploration to lessen the THD and to work the circuit in proficient way. The proposed research is sorted out in six segment: Objectives of Buck-Boost converter is looked into in Section 1. Schematic circuit of BBDCLCMLIFIM framework is described in Section 2. Different exchanging topology have explored in Section 3. Experimental

and Mathematical displaying of BBDCLCMLIFIM framework are carried in Section 4, and Section 5 concludes up this paper.

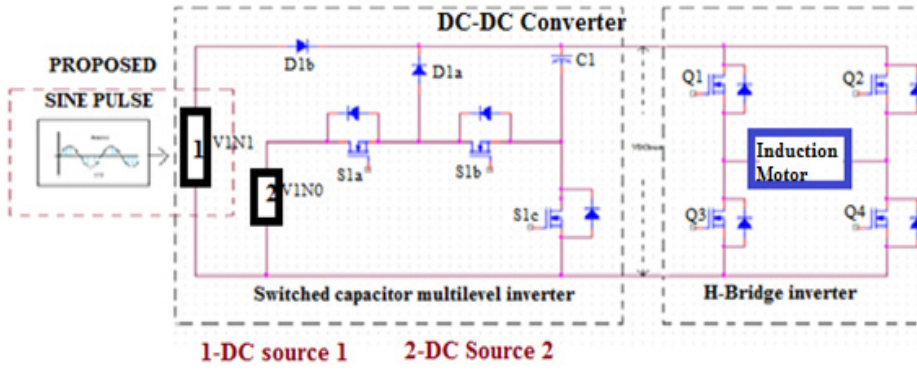


Fig. 4. Proposed circuit diagram of BBDCLCMLIFIM with Induction motor

2. Materials and methods

Modeling structure of BBDCLCMLIFIM.

BBDCLCMLIFIM contains double unbalanced DC voltage sources, buck support converter unit, DC-interface module (DCLM) and H-bridge inverter. H-bridge inverter is associated in parallel to the DC-interface framework.

2.1. Buck-boost Cuk DC-link configuration

Buck Boost (BB) converter unit is associated with topsy-turvy DC sources. The identical structure of BDCLMLI is appeared in Fig. 4.

Number of levels in BBDCLCMLIFIM arrangement is determined as:

$$R_{level} = 2(P+1)S - 1. \quad (1)$$

Number of switches in BDCLCMLI is given by (2):

$$R_{Switch} = 2S + 4P + R, \quad (2)$$

where R_{level} is the quantity of levels, R_{Switch} is the quantity of switches in BBDCLCMLIFIM, Q-number of H-bridge inverter, S-number of DC sources and P-number of buck-help units.

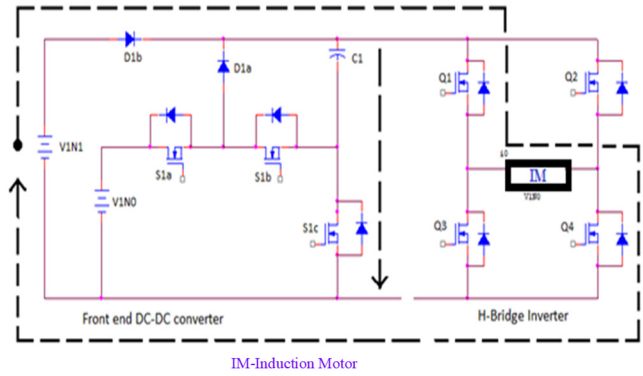
2.2. Modes of operation

Mode 1: Output voltage = $\pm V_{IN1}$ state.

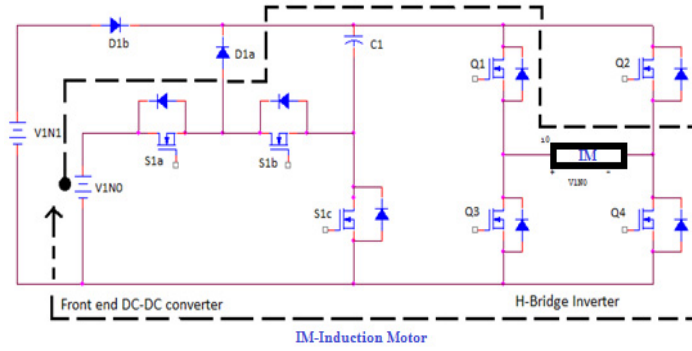
Capacitor C_1 is charged to the information voltage V_{IN1} through D_{1b} by turning ON transistor S_{1c}. Transistors S_{1a}, S_{1b} and diode D_{1a} stay turned off. The DC voltage at this state is equivalent to V_{IN1} as V_{IN0} is closed by turning off transistor S_{1a}. Voltage source V_{IN1} alone supplies capacity to the heap. Fig. 5(a) delineates the identical circuit for V0 = $+V_{IN1}$.

Mode 2: Output voltage = $\pm V_{IN0}$ state.

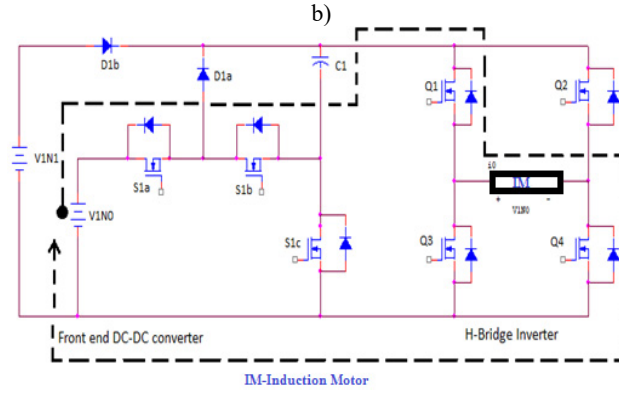
For typical activity of the proposed inverter, $V_{IN0} > V_{IN1}$. In the DC-DC converter, just transistor S_{1a} is turned ON while different transistors are turned off. Consequently, V_{IN0} is associated with the DC bus through diode D_{1a}. As $V_{IN0} > V_{IN1}$, diode D_{1b} is turn around one-sided and henceforth squares V_{IN1}. Fig. 5(b) delineates the proportionate circuit for $V_0 = +V_{IN0}$. The capacitor C_1 is open at this state. Along these lines, its voltage stays at V_{IN1}.



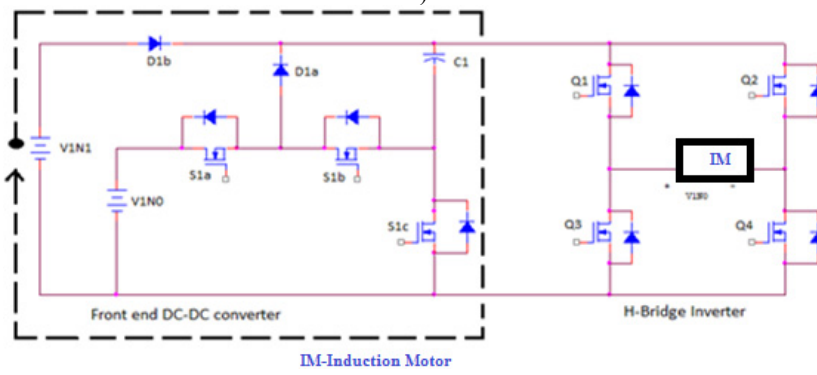
a) IM-Induction motor



b)



c)



d)

Fig. 5. Operating modes of proposed BBDCLCMLIFIM

Mode 3: Output voltage = $\pm(V_{IN0} + V_{IN1})$ state.

Capacitor C_1 charged to V_{IN1}, is associated in arrangement with info voltage source V_{IN0} by turning ON transistors S_{1a} and S_{1b}. Diode D_{1b} is turn around one-sided and blocks V_{IN1}. The net voltage that shows up over the DC transport currently is equivalent to $V_{IN0} + V_{IN1}$. In this state, input voltage source V_{IN0} and capacitor C_1 supply capacity to the heap. Fig. 5(c) delineates the proportionate circuit for $V_0 = +(V_{IN0} + V_{IN1})$.

Mode 4: Output voltage = 0 V state.

To acquire zero dimension at the output after the positive half cycle Fig. 5(d), just transistor Q_1 is turned ON, while the various switches in the H-bridge inverter stay killed. The diode of transistor Q_2 is utilized for nothing wheeling. Essentially, to get zero dimension at the output after the negative half cycle, just transistor Q_4 is turned ON, while the various switches in the full scaffold inverter stay turned off. For this situation, the diode of transistor Q_3 is utilized for freewheeling. The switches in the front-end converter stay in their past states.

(a) Mode 1: Output voltage = $\pm V_{IN1}$ state (b) Mode 2: Output voltage = $\pm V_{IN0}$ state.

(c) Mode 3: Output voltage = $\pm(V_{IN0} + V_{IN1})$ state (d) Mode 4: Output voltage = 0 V state.

At Output voltage = $\pm V_{IN1}$, the net voltage that shows up over the DC transport currently is equivalent to $V_{IN0} + V_{IN1}$.

The output voltage is communicated as:

$$OUT_{dC1} = C_1 I_1 - \frac{I_2}{\pm V_{IN1}}. \tag{3}$$

At right now charging vitality is given as:

$$CE_{i1} = OUT_{dC1} I_{sa} \bullet \pm V_{IN1}. \tag{4}$$

The normal output voltage of buck help converter can be communicated utilizing Eq. (5):

$$Outbb = OUT_{dC1} + \pm V_{IN1}. \tag{5}$$

The vitality discharged by the circuit at switch s1a by the proposed converter given by Eq. (6):

$$CE_{i1} = (Out_{bb} - OUT_{dC1}) Is_{1a} \pm V_{IN0}. \tag{6}$$

The proposed converter BB with lessening exchanging misfortunes are communicated in condition Eq. (7):

$$OUT_{BB} = (Out_{bb} - OUT_{dC1}) Is_{1a} \pm V_{IN0}(1 - K_1). \tag{7}$$

Voltage variety over the capacitor C1 can be communicated by Eq. (8):

$$\Delta C_1 = OUTI_1 \frac{[V_{BB} - C_1(I_1 - I_2)]}{f} * C_1 * OUT_{BB}. \tag{8}$$

Operation modes 3 and 4: Capacitor C_1 charged to V_{IN1}, is connected in series with input voltage source V_{IN0} by turning ON transistors S_{1a} and S_{1b}. Diode D_{1b} is reverse biased and blocks V_{IN1}. To obtain zero level at the output after the positive half cycle only transistor Q_1 is turned ON, while all the other switches in the H-bridge inverter remain turned OFF. The diode of transistor Q_2 is employed for free-wheeling. Similarly, to obtain zero level at the output after the negative half cycle, only transistor Q_4 is turned ON, while all the other switches in the full extension inverter stay turned off. The net voltage that shows up over the DC transport currently is equivalent to $V_{IN0} + V_{IN1}$. are appeared in Fig. 5(c) and 5(d).

Capacitor C_1 charged to V_{IN1}, is associated in arrangement with info voltage source V_{IN0} by turning ON transistors S_{1a} and S_{1b} the present changes from I_3 to I_4. The voltage over the inverter circuit is communicated as:

$$OUT_{dc2} = C_2 I_4 - \frac{I_3}{V_{IN0}}. \tag{9}$$

The vitality discharged by the circuit at switch s_{1a} by the proposed converter given by Eq. (10):

$$CE_{i2} = (Out_{bb} - OUT_{dC1}) Is_{1c} \pm V_{IN0}. \tag{10}$$

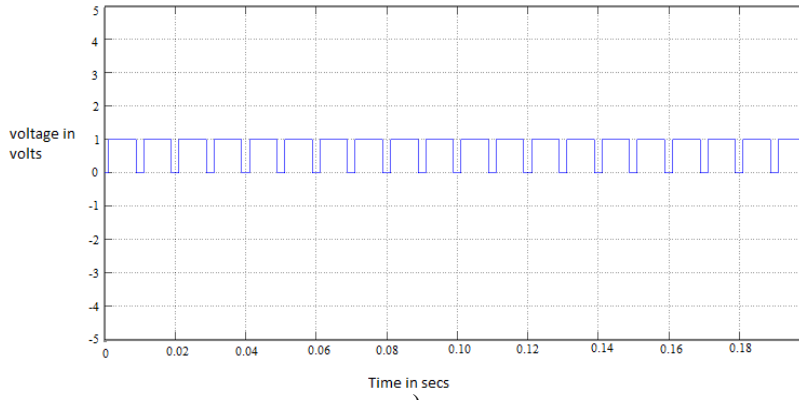
The normal output voltage of buck help converter II is acquired utilizing Eq. (11):

$$OUT_{bb} = pmdc_2 + C_2 V_{IN0} + V_{IN1}. \tag{11}$$

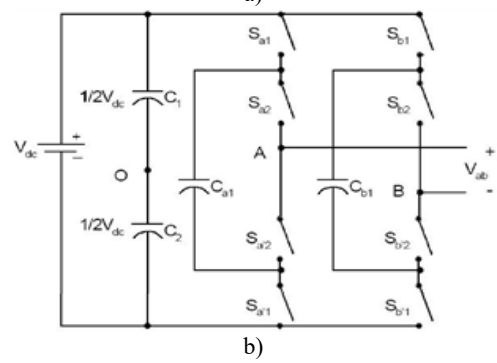
The proposed converter BB with lessening exchanging misfortunes are communicated in condition Eq. (12):

$$OUT_{BB} = (Out_{bb} - pmdc_2) Is_{1a} \pm V_{IN0}(1 - K_1). \tag{12}$$

A model of single-stage BBDCLCMLIFIM-based engine is structured and executed for 230 V (V_{max}) output voltage. The examples of PWM pulses, Simulink display and the output voltage utilizing n-levels are appeared in Figs. 6(a) and (b).



a)



b)

Fig. 6. a) PWM pulses, b) topology of a flying capacitor multilevel inverter

Rectifier units, buck boost converter units, controller units, driver units, DC-connection and H-bridge inverter units are incorporated in this model. The rectifier units are planned utilizing a

scaffold rectifier (MICBR1010) and a capacitive channel of 1000 μF. The outputs of rectifier units go about as the contribution for the lift chopper units and battery banks. The buck support converter are manufactured utilizing IRF840 controlled power gadgets (MOSFET) switches and aloof segments ($C_1 = C_2 = 100$ μF). The dspic gives control signs to the MOSFET driver circuit. The highlights of dspic are utilized to accomplish effective control of the proposed framework. The DCLM and H-bridge inverter frameworks are manufactured utilizing IRF840 control MOSFET switches. The experiment identical circuit of BBDCLCMLIFIM framework is appeared in Fig. 22. Output voltage across capacitor C_2 can be expressed by (13):

$$\Delta C_2 = OUTI_1 \frac{[V_{BB} - C_2(I_1 - I_2)]}{f} * C_2 * OUT_{BB}. \quad (13)$$

Table 1. Switch turning states of BBDCLCMLIFIM with respect to potential rating

Potential rating, Volts	State level	Switch turning states													
	–	S_{1a}	S_{1c}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
$+4V_{dc}$	1	0	1	0	1	1	0	1	0	1	0	1	0	1	0
$+3V_{dc}$	2	1	0	0	1	1	0	1	0	1	0	1	1	0	0
$+2V_{dc}$	3	1	0	0	1	1	0	1	1	0	1	1	0	1	0
$+1V_{dc}$	4	0	1	0	1	1	0	1	1	0	1	1	1	0	0
$+0V_{dc}$	5	1	0	0	1	1	0	1	1	0	1	0	1	0	1
$–0V_{dc}$	6	1	1	1	0	1	0	1	1	0	1	1	0	1	0
$–1V_{dc}$	7	0	1	1	0	1	0	1	1	0	1	1	1	0	0
$–2V_{dc}$	8	1	1	1	0	1	0	1	1	0	1	0	1	0	1
$–3V_{dc}$	10	0	1	1	0	0	1	0	1	0	1	1	1	0	0
$–4V_{dc}$	11	1	0	1	0	0	1	0	1	0	1	0	1	0	1
$+4V_{dc}$	12	1	0	0	1	1	0	1	0	1	0	1	0	1	0
$+3V_{dc}$	13	1	1	0	1	1	0	1	0	1	0	1	1	0	0

2.2.1. Operation of H-bridge inverter configuration

The output voltage before H-bridge inverter for single PWM pulse is appeared in Fig. 9. It delivers a most extreme voltage of total of V_{1N1} and V_{1N0}. At present, a couple of topologies with various control systems have been presented for cascaded staggered inverters. This exploration considered this H connects idea and executed in this framework. H-bridge inverter framework works in two activity modes. The positive half-cycle sizes of AC output voltage are communicated utilizing Eqs. (14)-(16):

$$OUT_1 = OUT_{bb}, \quad (14)$$
$$BB = OUT_{bb}, \quad (15)$$
$$OUT_o = OUT_{o1} + B_1 OUT_{bb}. \quad (16)$$

At MODE (b), the contrary half cycle of AC output voltage is incorporated by stimulating H-connect control gadgets S_{1c} and S_{1d} as appeared in Fig. 5(b) and (d).

The negative half cycle extents of AC output voltage are given by:

$$OUT_{o1} = -VOUT_{BB}, \quad (17)$$
$$BB = -VOUT_{BB}. \quad (18)$$

2.2.2. Buck boost converter conduction losses

With reference MOSFET switching losses are determined utilizing the exact voltage drop with arrangement straight resistor ($RD = 0.07$). It decides the terminal entryway by terminal source

voltage and intersection temperature. The misfortunes in the MOSFET switch are given in Eq. (19).

$P(condS_2) = I_{S_{1,2}}^2 \times RDS$ on:

$$I\left(S_{1,2}\right)^2 = D_2 \times \left[I\left(OS_{1,2}\right)^2 + \frac{\Delta I\left(OS_{1,2}\right)^2}{12}\right], \tag{19}$$

where $(Is_{1,2})$ shows the present coursing through the switch (S_1), (S_2) represents the "ON" time of switch and delta I_2 represents the normal swell current of switch. Exchanging ampere decided as $(I(O_{S2}))$ is gotten from Eq. (20). Initial current $\Delta I_{S_{1,2}}$ are given as in Eq. (20):

$$\Delta I(OS1,2) = \frac{I\left(OS_{1,2} - max\right) - \left(IOS_{1,2} - min\right)}{2} = \frac{8.53 - 6.6}{2} = 0.965, \tag{20}$$

where $(I(S_{1,2} - max))$ and $(I(S_{1,2} - min))$ gives high and low sizes of intensity controlled gadget current $(S_1\text{-}S_8)$ as outlined in Fig. 7. From Fig. 8, $D2 = 0.22$, $I_{S_2} = 7.565$ and $\Delta I_{OS_{1,2}} = 0.965$, which are substituted in Eq. (21), total ripples and losses are gotten from MOSFET switches [18] as settled and conduction losses are determined in Eq. (21), (22):

$$I\left(S_{1,2}\right)^2 = 12.58 \text{ A}, \tag{21}$$

$$P\left(\text{cond}S_{1,2}\right) = 12.58 \times 0.069 = 0.90 \text{ W}. \tag{22}$$

Power devices conveyance losses $(S_{1,2})$ during starting.

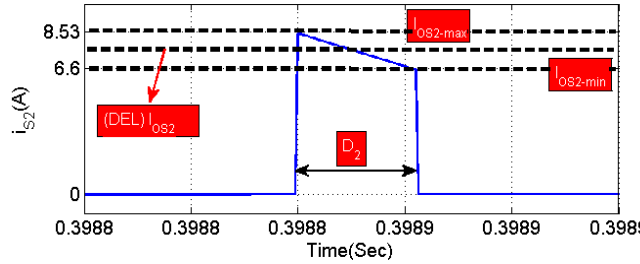


Fig. 7. Conduction of power devices at open loop condition [18]

3. Results and discussions

3.1. Simulation performance evaluation

The designed control topology is striving with a perfect three-stage connection with a two-phase BBC power supply and an induction motor. Table 2 shows the simulation specifications, which supports in reducing the harmonic distortion.

3.2. Output voltage before H-bridge inverter for single pulse

The output voltage before H-bridge inverter for single PWM pulse is shown in Fig. 9. It produces a maximum voltage of sum of V_{1N1} and V_{1N0}.

3.3. Output voltage and current for single PWM pulse

The output voltage and current of multilevel inverter for single pulse input is shown in Fig. 10 and Fig. 11.

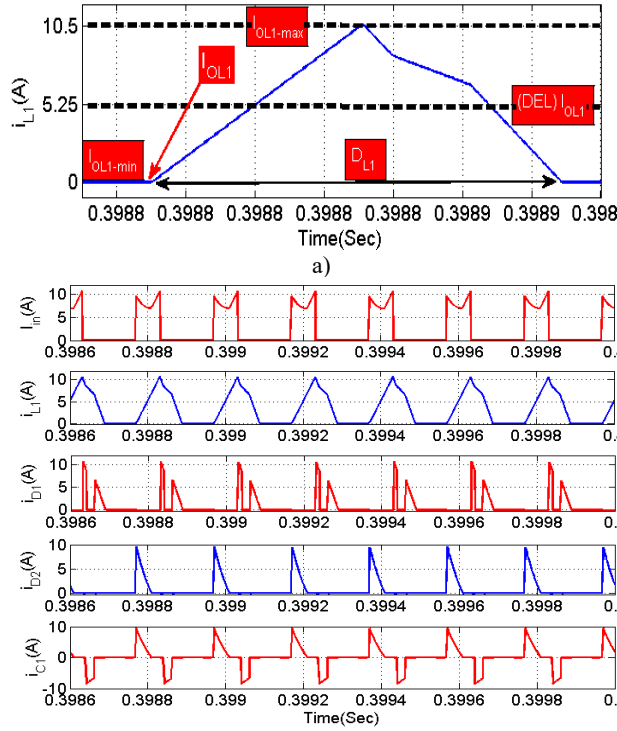


Fig. 8. Converter: a) diode conduction losses b) ripple currents across inductor, diodes and capacitor [17]

Table 2. Simulation specifications

PARAMETERS	UNITS
Solar PV voltage	24 V
Solar PV current	2.20 A
Solar PV power	74 W
FET resistance (Ron)	0.1 Ω
Internal diode resistance (Ron)	0.01 Ω
Internal diode inductance (Lon)	1 H
Internal diode forward voltage (V_f)	1 V
Initial current (I_c)	0.1 A
Snubber resistance (R_s)	1×10^{-5} Ω
Snubber capacitance (C_s)	1 nF
Inductance (Lon)	1 H
Forward voltage (V_f)	0.8 V
Initial current (I_c)	1 A
Snubber resistance (R_s)	500 Ω
Snubber capacitance (C_s)	250×10^{-9} nF

The output waveform with seven steps produces a staircase wave which reduces the harmonic distortion. Single pulse multilevel inverter is an existing system. To improve the performance the single pulse is replaced by sine pulse. Our proposed system has sine signal compared with ramp signal as an input pulse. It reduces harmonic distortion than single pulse. The simulation outputs for sine pulse are given below. The multilevel inverter switches receives the converter outputs. The recreation parameters of the designed model are set as follows: input voltage = 480 V, input current = 27 A, input supply frequency = 50 Hz, exchanging frequency = 2 kHz, resistance =20 Ω and inductance = 310 mH for 7 level inverter. The output voltages are synthesized using the

MATLAB platform. Multilevel inverters with 7-levels output voltage synthesis are shown in Fig. 13, 14 and 15.

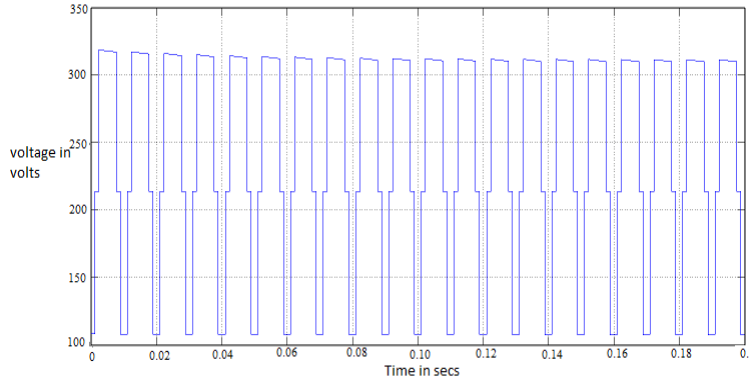


Fig. 9. Output voltage before H-bridge inverter

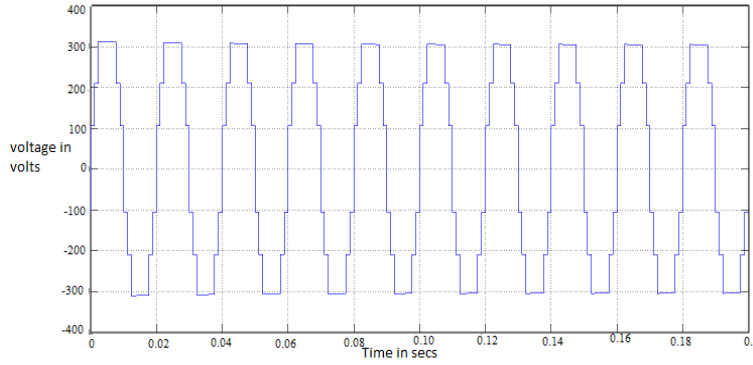


Fig. 10. Output voltages after H-bridge inverter

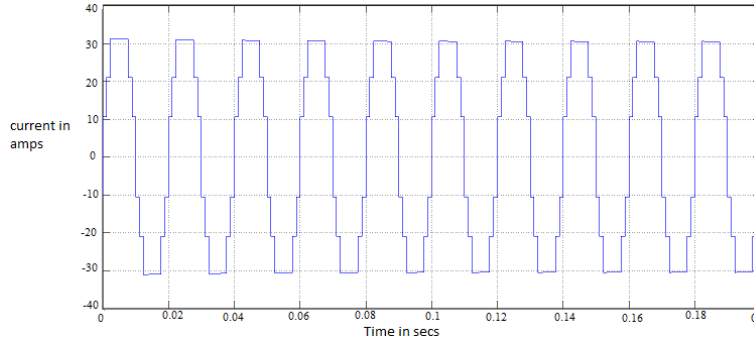


Fig. 11. Output current after H-bridge inverter

3.4. Voltage across capacitor for sine pulse

Capacitor gets charged and maintains it ideally and then it gets discharged. The voltage across the capacitor for sine pulse modulation is shown in Fig. 12.

3.5. Output voltage before H-Bridge inverter

The output voltage before H-bridge inverter for sine PWM pulse is shown in Fig. 13. It produces a maximum voltage of sum of V_{1N1} and V_{1N0}.

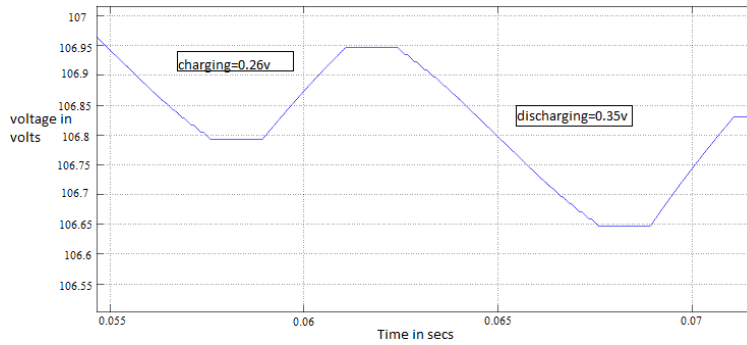


Fig. 12. Voltage across capacitor for sine PWM

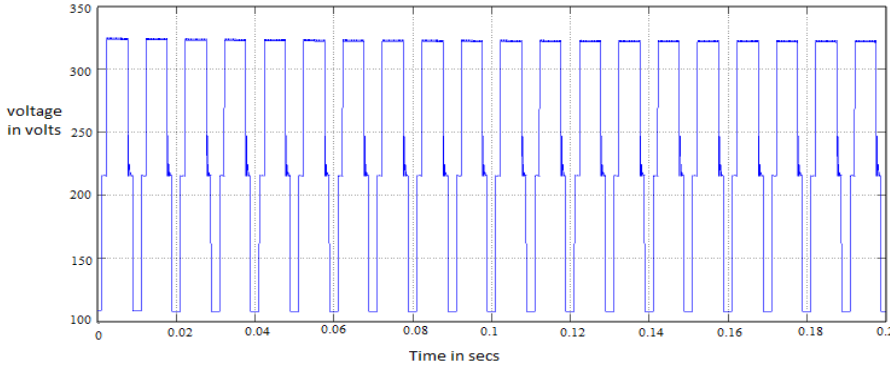


Fig. 13. Output voltage before H-bridge inverter

3.6. Output voltage and current for sine PWM pulse

The output voltage and current of multilevel inverter for sine pulse input is shown in Fig. 14 and Fig. 15.

The output waveform with seven steps produces a staircase wave which reduces the harmonic distortion.

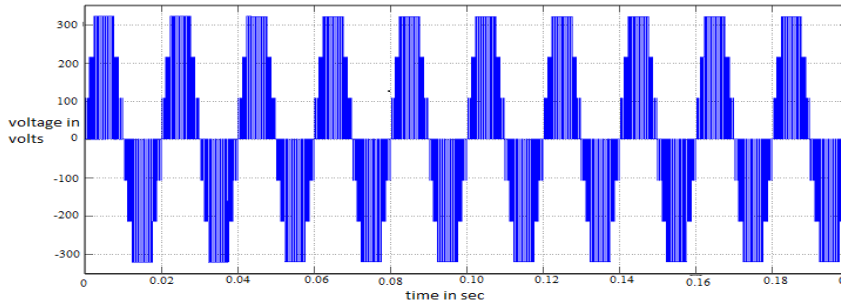


Fig. 14. Output voltage after H-bridge inverter

3.7. THD analysis

The THD % for single pulse and sine pulse at modulation index 1 are shown in Fig. 16.

THD for various modulation indices.

The comparisons of THD percentage of single pulse and sine pulse for different modulation indices are tabulated in Table 3.

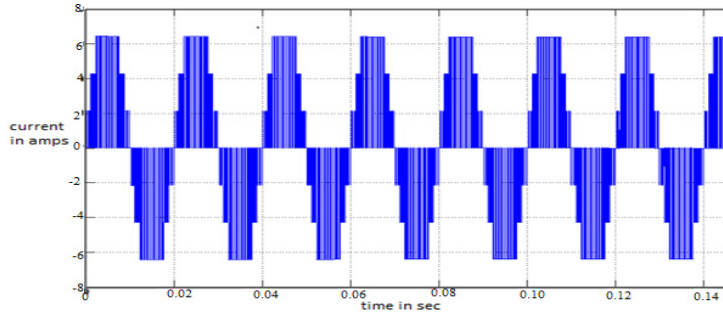
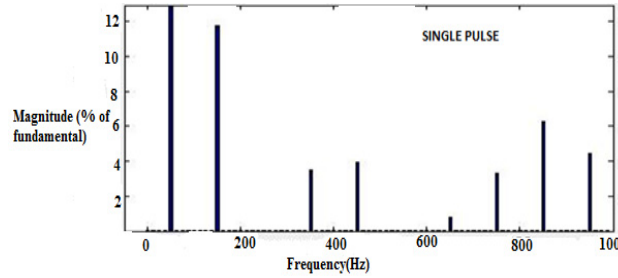
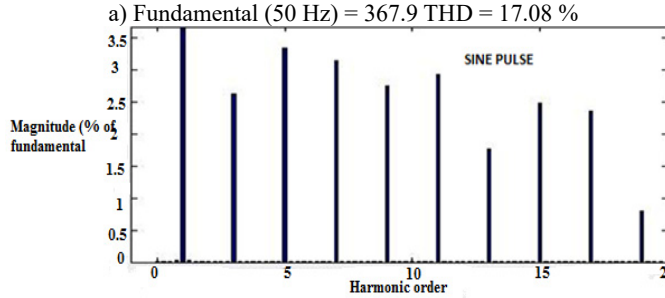


Fig. 15. Output current after H-bridge inverter



a) Fundamental (50 Hz) = 367.9 THD = 17.08 %



b) Frequency (50 Hz) = 282.1 THD = 8.11 %

Fig. 16. a) THD results for single pulse, b) THD results for sine pulse

Table 3. Comparison of THD percentage of single pulse and sine pulse for different modulation indices

Sl. No	Modulation index	Conventional	Proposed
		THD %	THD %
1	1.2	20.64	8.45
2	1.1	18.85	8.80
3	1	17.08	8.11
4	0.9	15.84	8.33
5	0.8	16.30	10.63
6	0.7	20.99	14.94
7	0.6	23.95	14.24
9	0.4	28.98	20.36
10	0.3	48.32	18.17

3.8. Analysis of speed regulation in pumping process of RO section in textile wastewater treatment

The block diagram of speed control system is shown in the Fig. 17.

The pumping process parameters, pressure and flow are optimized by adjusting the electrical parameters, duty cycle and speed. The proposed Fuzzy Logic Control (FLC) system has two inputs:

the first input is the difference in actual and desired flow; the second input is the difference in actual and desired pressure. FLC is applied to the speed controlling system to control the speed of the induction motor. The output of FLC is sent to the three-phase inverter to produce waveform with variable frequency to control the speed of the three phase induction motor. For fuzzy logic controller, ranges for membership functions have to be defined. The range of input variables pressure (PR), flow (FL) and output variable duty cycle are defined as Negative Large (NL), Negative Medium (NM), Negative Small (NS), Zero (ZE), Positive Small (PS), Positive Medium (PM), Positive Large (PL). The output variable is used to calculate the needed change of frequency which will be used to control the speed of induction motor. All fuzzy rules used in the proposed system are summarized in the Table 4.

Fig. 18 shows the fuzzy membership function of fuzzy controller for speed controlling system with inputs and output of the system.

Table 5 shows the variation of electrical parameter values with respect to process parameters.

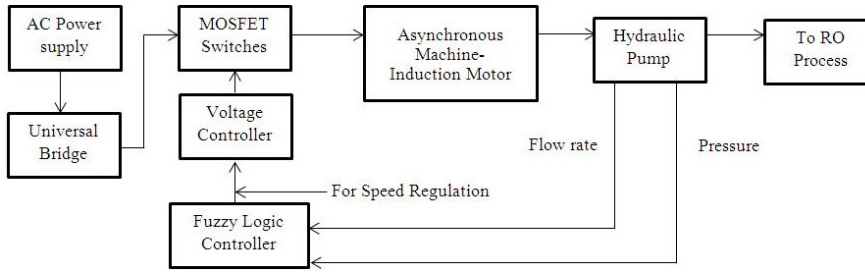


Fig. 17. Block diagram of speed control system

Table 4. Fuzzy rules for speed control system

PR / FL	NL	NM	NS	ZE	PS	PM	PL
NL	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PL	ZE	PS	PM	PB	PB	PB	PB

Table 5. Variation of electrical parameter values with respect to process parameters

Outflow of liquid from pump (gpm)	Discharge pressure of liquid from pump (psi)	Duty cycle for inverter	Speed of induction motor (rpm)
400	21	0.1	1750
219	18.67	0.2	1051
188	15.98	0.3	900
100	11	0.5	690

Whenever there is a deviation of process parameter value from set point, fuzzy controller takes immediate control action by sensing the change of values. By changing the duty cycle, frequency of the supply that is fed to the inverter is varied. Consequently, the rotor speed can be varied. Instead of running the motor at full frequency of 50 Hz during the entire day, the frequency can be reduced when the load reduces, and energy consumption can be reduced. Fig. 19 shows the rotational speed of rotor in rpm. The speed of the motor obtained for the corresponding pressure and flow is 900 rpm.

Fig. 20 and Fig. 21 shows the discharge flow rate and discharge pressure of the pumping process. The obtained flow and pressure values are 188 gpm and 15.98 psi for 900 rpm.

Fig. 18. Membership function for speed controller

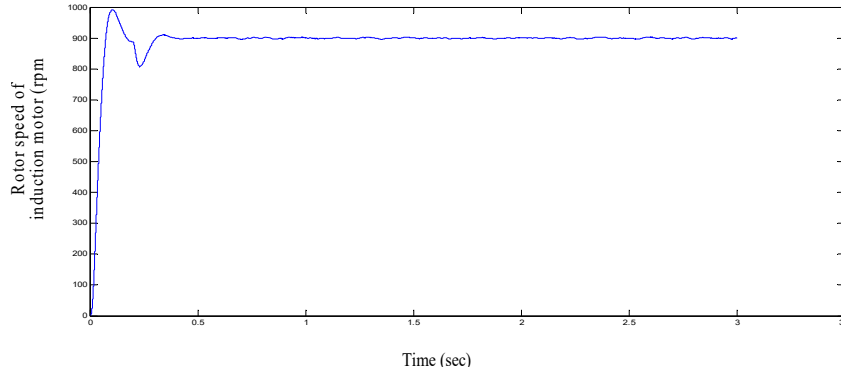


Fig. 19. Rotor speed of the motor

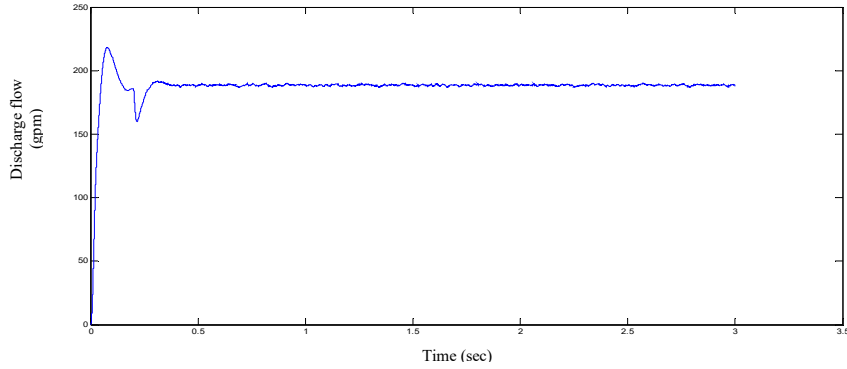


Fig. 20. Discharge flow rate of the pump

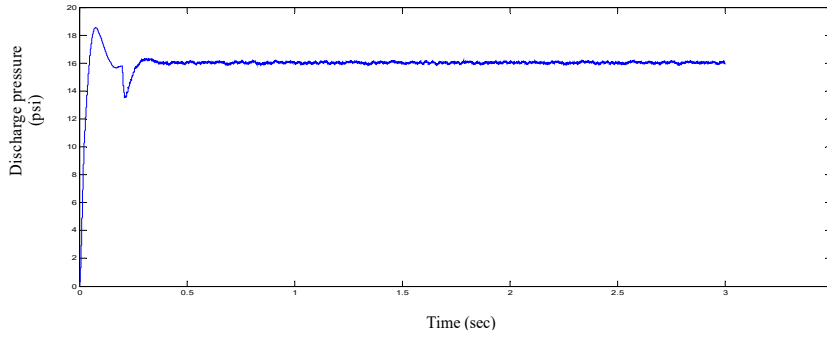


Fig. 21. Discharge pressure of the pump

Whenever there is a deviation of process parameter value from set point, fuzzy controller takes immediate control action by sensing the change of values. By changing the duty cycle, frequency of the supply that is fed to the inverter is varied. Consequently, the rotor speed can be varied. Instead of running the motor at full frequency of 50 Hz during all the day, the frequency can be reduced when the load reduces, and energy consumption can be reduced.

3.9. Experimental evaluation

The converter outputs are encouraged to staggered inverter switches for the application for the material water siphoning process with the fluffy rationale controller. The experimental parameters are set as pursues: supply recurrence = 50 Hz, input voltage = 480 V, input current = 27 A, trading recurrence = 2 kHz, opposition = 20 Ω, inductance = 310 mH. Table 6 demonstrates engine parameters. The acknowledgment equipment circuits are appeared in Fig. 22. Block diagram and Prototype Model equipment of BBDCLCMLIFIM appeared in Fig. 23 and 24. The structured BBDCLCMLIFIM analysis were carried out and hence the proposed method achieves reduced THD which is more cost effective and efficient for the various industry applications.

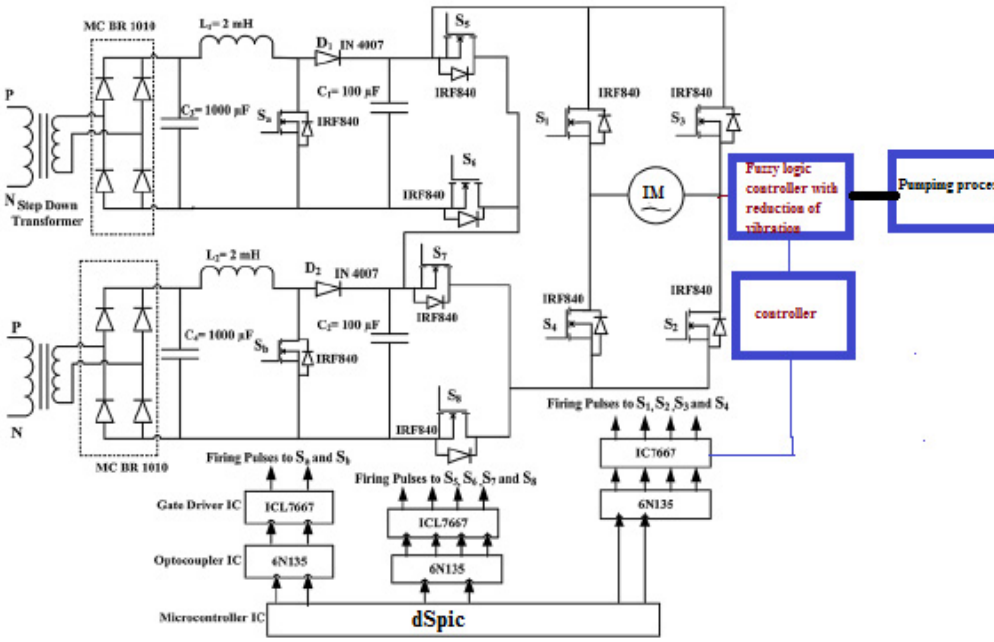


Fig. 22. Realization of hardware circuit diagram of BBDCLCMLIFIM

Table 6. Various type of equipment with their range specification

S. No	Type of the equipment	The range
1	Battery	12 V/4.7 AH
2	Step down transformer	230 V/12 V
3	Step down transformer	230 V/5 V
4	MOSFET	IRF840
5	Induction motor	220 V, 100 A, 1200 rpm

Table 7. Comparison of THD for various multilevel inverters to reduce vibration across the induction motor

Parameter	Diode clamped	Developed H bridge	Torque ripple	Current ripple
Proposed THD for level 7 (%)	17.08	8.11	0.6	0.7
THD for level 5 (%)	15.84	8.33	0.66	1.2
THD for level 3 (%)	16.30	10.63	0.71	1
THD for level 2 (%)	20.99	14.94	0.89	1.6

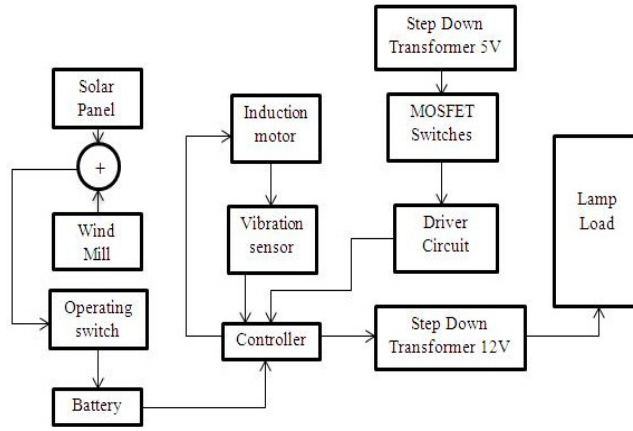


Fig. 23. Experimental block diagram of BBDCLCMLIFIM

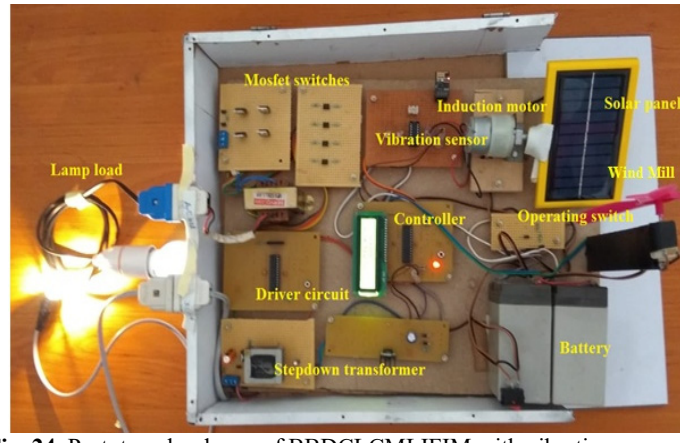


Fig. 24. Prototype hardware of BBDCLCMLIFIM with vibration sensor for pumping applications in textile wastewater treatment

4. Conclusions

The hybrid quasi converters with solar and battery sources are incorporated in the proposed subsystem, for analysis and design. The task manages cascaded H-connect staggered inverter that can be utilized for both single and three stage change. The structure is created with H-bridge inverter including DC-DC converter. A sine pulse width twist is decided on PWM pulses. The inverter essentially takes care of the issue of capacitor voltage adjusting as every capacitor is charged to the esteem equivalent to one of the information voltages at each cycle. Recreation is finished with the assistance of MATLAB Simulink programming and the exploratory outcomes for current and voltage at various THD esteems are appeared and the equivalent is done for equipment. The proposed method is designed with 7-level diodes clamped based on the converter unit. The H bridge topology was developed with MATLAB/Simulink. Finally, the operation of total subsystem is verified based on the harmonic reduction. From the experimental results, it is concluded that the proposed subsystem with the developed H bridge converter has the least total harmonic distortion as 8.11 % and 17.08 % for 7-level and 5-level MLI topology respectively. The prototype structure is conceded and analysed for various parameters of proposed method, which results in reduced switches and proves more efficient than other conventional methods and in addition it is more proficient for pumping process in textile industry for wastewater treatment.

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