2754. Design and implementation of DC source fed improved dual-output buck-boost converter f[or](https://crossmark.crossref.org/dialog/?doi=10.21595/jve.2017.19228&domain=pdf&date_stamp=2017-12-31) agricultural and industrial applications

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DOI https://doi.org/10.21595/jve.2017.19228

Abstract. The proposed research involves, a design and implementation of DC source fed improved Dual output Buck-Boost converter for agricultural and industrial applications. It consists of step up and step-down converter, DC-link module. Compared with conventional two converters, the designed system results in reduction of voltage tension across the switches, compact power switches, DC source reckoning and reduced inrush current. DC-link switching is achieved by reduced ripple voltage which results in improved quality of obtained output power. Reduction in switch count makes the system more cost effective. In addition, the motor speed is regulated by PI controller. Brushless DC Motor produce torque ripple and cause mechanical vibration, acoustic noise due to structural imperfectness and control system, to overcome this suppression control method of vibration for brushless DC motor utilizing feedforward compensation with Fourier transform utilizing a vibration signal acquired by an acceleration sensor attached to the motor frame is proposed. A simulation and prototype model of Dual output Buck-Boost converter is developed, and its performance is analysed for various operating conditions.

Keywords: DOBB, symmetrical/asymmetrical, ripple voltage, efficiency, losses, vibration, Fourier transform.

1. Introduction

1.1. Single stage multiport converter

By combating with the challenges of global warming, clean energies, like fuel cell, PV and wind energy have been highly encouraged because of its high their efficiency. Owing to the electrical properties of clean energy, the power generated is severely impacted by the climate or it has transient responses that are slow, and the output voltage is easily affected by load changes [1]. Further, the other auxiliary components, like storage elements, control boards and so on are generally necessary to guarantee the right operation of clean energy [2]. Therefore, different voltage levels are needed in the power converter of a clean energy generation system. Generally, several single input single output (SISO) DC-DC converters with diverse voltage gains are integrated to meet the demands of different voltage levels, such that their system control is more complex and the respective cost is high [3]. The synthesis of multiport converters can be done by connecting different SISO converters to one common dc bus as illustrated in Fig. 1. Though common in traditional hybrid power systems, such kind of configuration can result in a sophisticated structure and huge cost. The inspiration behind the present study is to develop a single input multi output (SIMO) converter for maximizing the conversion efficiency and voltage gain, decreasing the control complexity and helping to save the manufacturing expense of the converter.

SIMO converters can be divided into isolated and non-isolated configurations. In the case of isolated topologies, a transformer with multiple secondary windings acts as an interface between the input and output ports. Only one output voltage generally the one with the heaviest load is

controlled while the others are decided by means of the turn ratios of the secondary windings. Therefore, independent output voltage regulation is not a direct impression, and this is not a cost-efficient solution also [4]. The non-isolated SIMO topologies can be further divided into independent- and series-output configurations. With the independent-output configuration [5, 6], every output port shares the same ground and decreases the number of external heavy components like inductors and power switches, resulting in reduced expense and losses in the system. However, in these configurations, loads are constructed independently as illustrated in Fig. 2(a).

Fig. 1. Conventional multiport converter architecture

In a similar manner in the series-output configuration [7, 8], as indicated in Figs. 2(b) and (c), various outputs are connected serially. Series regulated DC voltages might be necessary in several low- and high-power applications. One among the most remarkable applications of this new family of DC-DC converters is the boosting and regulation of the low and variable output voltage of renewable energy for the DC link of grid/load connected systems on the basis of inverters. Therefore, Series-output SIMO converters are considered to be effective solutions in balancing the dc-link voltage of loads in an effective manner [9].

Nami et al. [6] have introduced a novel DC–DC multi-output boost converter that can share its total output between the different series of output voltages used in low- and high-power applications. Unluckily, nearly two switches for one output are needed, and DC-DC multi-output control mechanism was complex. In addition, the associated output power cannot provide individual loads in an independent way. Boora et al. [8] also have illustrated a novel multi-output DC-DC converter topology, which has the capabilities of step-up and step-down conversion. In this topology, multiple output voltages could be produced and could be utilized in varied applications like multilevel converters with diode-clamped topology or power supplies with different voltage levels, but the multiple number of switches in the converter results in power losses. Patra et al. [10] have introduced a SIMO DC-DC converter with the capability of producing buck, boost, and inverted outputs simultaneously. Nonetheless, approximately three switches for one output are needed for SIMO.

In addition, in this research paper, we propose a suppression control method for torque vibration of brushless DC motors utilizing the acceleration sensor, the Fourier Transformer and the repetitive controller. In the proposed system, only one frequency component of vibration signal from acceleration sensor is inputted to repetitive controller, the stability of the control system can be improved. Approximate analysis is performed to study the stability of the repetitive control system. In order to realize online generation of feedforward compensation signals to reduce the vibration, auto-tuning method of the repetitive control parameters is also presented.

The periodical torque ripple occurs synchronously with the motor rotation. And also, the repetitive controller has large loop gain (basically infinity) only for the fundamental repetitive frequency component and its harmonics. For the above reasons, the repetitive control system is effective to reduce the vibration due to periodical torque ripples.

Fig. 2. Non-isolated SIMO: a) boost converter independent output configuration [7], b) boost converter series output configuration [7], c) BB converter series output configuration [8], d) schematic diagram of control system

However, because the vibration signals detected by the acceleration sensor contain various frequency components and the mechanical system around the motor and load has complicated resonant characteristics, we cannot stabilize the repetitive control system and reduce the vibration by directly using the vibration signals from sensor [11]. Then, we investigate the method which only one frequency component of the vibration signal is extracted from the vibration signals detected by the acceleration sensor, and the repetitive control is performed for every frequency component of the vibration. Generally, since the period of the vibration may not coincide with that of the power supply but may be multiple of that, we set the period of the vibration to $Tr (= NrT, T = f-1, f:$ motor driving frequency). For example, in the case of $Nr = 2$, the frequency components of the vibration are 0.5, 1.0, 1.5 and 0.5 is fundamental wave component of the vibration.

2. Materials and methods

2.1. Operation of the proposed DOBB converter

Fig. 3 illustrates the newly introduced single input multi-output topology that can carry out both of the step up and step-down conversions. DOBB converter offers versatility due to its capabilities in improving the dynamic response during the input voltage and load disturbances. Moreover, for applications where in there is a prior information or predictability regarding the load or input voltage disturbance, DOBB possesses the capability to eliminate the impact of these disturbances from the output voltages. Further, the new topology might act as sign priorities to the output voltages in order to attain a better dynamic performance in which the sensitive loads are provided in addition to loads that frequently vary.

Fig. 3. Proposed DOBB converter

In the present research, a DOBB converter topology is suggested with the following significant features.

• Any number of passive loads could be included.

• DOBB can work both in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM).

• The power supplied by input DC source can be controlled; therefore, the power budgeting between input energy source and load can be combined.

• DOBB uses only a single inductor that can help in reducing the complexity and the expense of the system in addition to simplifying the current sensing.

• The output voltages can be greater compared to the maximum input voltage or lesser in comparison to the minimum input voltage.

• Possibility of a symmetrical or asymmetrical voltage balancing of output capacitor voltage is present in this DOBB converter.

In Fig. 3, the new converter with Single-Input Two-Output is illustrated. This circuit comprises a BB switch (S_1), power sharing switch (S_2), two power diodes (D_1 and D_2), a single BB inductor (L_1) , intermediate capacitor (C_1) and output capacitors $(C_{01}$ and $C_{02})$ with two different kinds of loads $(R_1 \text{ and } R_2)$. As shown in the above figure, (R_1) and (R_2) refer to the model of load resistances, which can indicate the equivalent power supplying 40 W load. Two power switches, S_1 and S_2 , in the converter structure act as the chief controllable elements, which regulate the power flow and the output voltages of the converter. For every switch, a certain responsibility are given. The BB switch (S_1) is active in order to control the inductor (L_1) current to the value desired. Actually, S1 controls the capacitor (C_{01}) voltage to the necessary value by regulating the inductor (L_1) current. Control of the total output voltage $(V_{out} = V_{01} + V_{02})$ to necessary value is the responsibility of the power sharing switch (S_2) . Gate signals of switches and the current waveforms of inductor, switches, diodes and capacitors are illustrated in Fig. 4.

Based on the states of the switches, there are three various operation modes in the whole switching period as shown below.

Fig. 4. Key waveforms of the proposed DOBB converter

2.1.1. Switching state 1 [0 to t_0 (or) t_1 to t_2]

In switching state 1, the switch (S_2) is turned ON. As (S_2) is ON, diodes $(D_1 \text{ and } D_2)$ are reverse biased, therefore the switch (S_1) is turned OFF. The equivalent circuit of the new converter in this state is illustrated in Fig. 5. In this switching state, an inductor (L_1) current charges the capacitor (C_1) so that the inductor current reduces and capacitor (C_1) current faces a rise. Moreover, in this mode, capacitors (C_{01} and C_{02}) get discharged and supply their stored energy to the load resistances $(R_1$ and $R_2)$ correspondingly as illustrated in Fig. 4. In this mode the inductor and capacitor current and voltage are expressed by Eq. (1) below:

$$
L_{1} \frac{di_{L1}}{dt} = -V_{C1}, \quad C_{01} \frac{dV_{01}}{dt} = -\frac{V_{01}}{R_{1}}, \quad C_{02} \frac{dV_{02}}{dt} = -\frac{V_{02}}{R_{2}}.
$$
\n(1)\n
$$
\frac{\frac{i_{C1}}{R_{1}} - \frac{i_{C1}}{R_{1}}}{\frac{1}{R_{2}} - \frac{1}{R_{1}} + \frac{1}{R_{2}} - \frac{1}{R_{2}}}} = -\frac{V_{02}}{R_{2}}.
$$
\n(2)\n
$$
\frac{1}{\left(\frac{1}{R_{1}} - \frac{1}{R_{1}}\right)} = -\frac{V_{02}}{R_{2}}.
$$
\n
$$
V_{01} \frac{1}{\left(\frac{1}{R_{1}} - \frac{1}{R_{1}}\right)} = \frac{V_{02}}{V_{01}}
$$
\n
$$
V_{11} \frac{1}{\left(\frac{1}{R_{1}} - \frac{1}{R_{1}}\right)} = \frac{V_{02}}{V_{01}}
$$
\n
$$
V_{12} \frac{1}{\left(\frac{1}{R_{1}} - \frac{1}{R_{1}}\right)} = \frac{V_{01}}{V_{01}}
$$
\n(1)

Fig. 5. Switching state 1 [0 to t_0 (or) t_1 to t_2]

2.1.2. Switching state 2 $[t_0$ to $t_1]$

In switching state 2, switch (S_1) is turned ON. As (S_1) is ON, diode (D_2) gets forward biased so that the switch (S_2) is turned ON/OFF. The equivalent circuit of the converter proposed in this

 l

state is illustrated in Fig. 6. In this state of switching input DC source (V_{in}) charges the inductor (L_1) , and hence the inductor current sees an increase. At the same time, intermediate capacitor (C_1) and input dc source (V_{in}) delivers/discharges its energy to the output capacitor (C_{02}) through diode (D_2) . In addition, in this mode, capacitors $(C_{01}$ and C_{02}) get discharged and their stored energy is delivered to the corresponding load resistances $(R_1 \text{ and } R_2)$ as illustrated in Fig. 4. In this mode, the current and the voltage of the inductor and capacitors are expressed as in Eq. (2) below:

Fig. 6. Switching state $2[t_0 \text{ to } t_1]$

2.1.3. Switching state 3 $[t_2 \text{ to } t_3]$

In switching state 3, both the switches (S_1 and S_2) are turned OFF. Therefore, the diode (D_1) is forward biased. The equivalent circuit of the new converter in this state is illustrated in Fig. 7. In this switching state, an inductor (L_1) current charges the capacitor (C_{01}) , hence the inductor current reduces and capacitor (C_{01}) current rises. In addition, in this mode, capacitors (C_{01} and C_{02}) get discharged and supply their stored energy to the respective load resistances (R_1 and R_2) as illustrated in Fig. 4. The current and voltage of the inductor and capacitors are expressed by Eq. (3) below:

$$
L_1 \frac{di_{L1}}{dt} = -V_{01}, \quad C_{01} \frac{dV_{01}}{dt} = i_{L1} - \frac{V_{01}}{R_1}, \quad C_{02} \frac{dV_{02}}{dt} = -\frac{V_{02}}{R_2}.
$$
 (3)

From the above Eqs. (1), (2) and (3) it is noted that the capacitor, inductor charges/delivers the voltages at different switching modes of operation.

2.2. Control strategy of DOBB converter

The control mechanism is designed in order to achieve a stable voltage and control current storage capability of the topology in order to improve the dynamic response of the converter during the application of the load or input voltage disturbances. In the situation of rise in input voltage or drop in load current that may result in over-voltage in the output, closed loop regulation that senses the actual output voltage of the system and then activates the power switches in order to deviate the inductor current from the load and to eliminate the over-voltage is required. The case of drop in input voltage or rise in load current is also solved by using of closed loop control strategies. The contribution done by the present research depends up on the SIMO DOBB converter by selecting a classical Proportional Integral (PI) controller for a closed loop control strategy. The PI controller attempts to precise the error among the measured process variables and the desired set point through calculation and then provides an accurate output, consequently it can control the conversion process.

The PI controller computation involves two unique modes: proportional mode and integral mode. In the proportional mode, the reaction to the current error is decided, but in the integral mode, the reaction based recent error is decided. The weighted sum of the two modes provides the output to be the corrective action to the control element. PI controller is widely applied in several industries due to its simple design and unsophisticated structure. PI controller algorithm can be run by Eq. (4) :

$$
output(t) = KPerr(t) + KI \int_{0}^{t} err(t)dt,
$$
\n(4)

where means $err(t) =$ set voltage-actual voltage.

A voltage follower approach is adjustable for controlling the DOBB converter when it operates with DCM. A dual voltage sensors, i.e. total output voltage and capacitor (C_{01}) voltage measurement sensors, is necessary for regulating output voltage of the DOBB converter. Fig. 8 presents a closed loop control of the DOBB converter. This control strategy comprises a voltage error generator, Output Voltage Controller (OVC), Capacitor Voltage Controller (CVC) and a PWM generator.

The error generator of OVC compares of the preferred output voltage (V_{out}^*) of DOBB converter with the original output voltage (V_{out}) for generating an error voltage (V_{ce1}), provided in Eq. (5). In the same way, the error generator of CVC does the comparison of this DOBB converter capacitor (C_{01}) voltage (V_{01}) with the original output voltage (V_{01}) so as to produce an error voltage(V_{ce2}), provided by Eq. (6):

$$
V_{e1}(k) = V_{out}^*(k) - V_{out}(k),
$$

\n
$$
V_{e2}(k) = V_{01}^*(k) - V_{01}(k),
$$
\n(5)

where 'k' indicates the kth sampling instance. This error voltage (V_{e1}) and (V_{e2}) is delivered to an OVC and CVC for generating a regulated total output voltage (V_{ce1}) , and regulated capacitor output voltage (V_{ce2}) , given in Eq. (7) and (8) respectively:

$$
V_{ce1}(k) = V_{ce1}(k-1) + K_p \{V_{ce1}(k) - V_{ce1}(k-1)\} + K_i V_{ce1}(k),
$$
\n(7)

$$
V_{ce2}(k) = V_{ce2}(k-1) + K_p \{V_{ce2}(k) - V_{ce2}(k-1)\} + K_i V_{ce2}(k),
$$
\n(8)

where K_p and K_i refer to the respective proportional and integral gains of the PI controller. At last, the generation of the PWM signals are done by making a comparison between the output of OVC and CVC with the high-frequency saw-tooth signal (V_{car}), that generates the gate signals (V_{gs1} and V_{as2}) to DOBB converter switches (S_1 and S_2).

Fig. 8. Closed loop control of DOBB converter

2.2.1. Estimation of power losses in DOBB converter

The efficiency of system is indirectly proportional to the total power losses. The total power losses, in the DOBB converter, are the conduction, switching, diode and inductor losses. Occurrence of the conduction losses is due to the declining voltage across the device as well as the current flow through the device striking in chorus. Switching losses are sustained by the concurrent occurrence of voltage and current on the device while switching. The key waveforms of DOBB converter are shown in Fig. 9. I_{in} , i_{L1} , i_{D1} , i_{D2} , and i_{C1} are the current through the input supply, inductor L_1 , diodes D_1 and D_2 , and capacitor C_1 respectively. Evaluation of these losses can be done using simplified device models.

2.2.2. Calculation of switching losses of BB switch (S_1) in DOBB converter

2.2.2.1. Conduction loss of switch (S_1)

To analyze the conduction loss of switch (S_1) , the device is simplified to be a stable voltage drop that is in series with a linear resistor (RDS on $= 0.07$). RDS on is based on the applied Gate Source Voltage (V_{GS}) and the junction temperature. The conduction loss of switch (S_1) is expressed in Eq. (9):

$$
P_{cond-S1} = I_{S1}^2 \times RDSon,
$$
\n⁽⁹⁾

where (I_{S1}) indicates the current flowing through the switch (S_1) , (I_{S1}) is further divided by the respective inductor current (I_{S1L1}) and capacitor current (I_{S1C1}) flowing through the switch (S_1) . The current conduction of switch (S_1) is expressed in Eq. (10):

$$
I_{S1}^2 = I_{S1L1}^2 + I_{S1C1}^2, \quad I_{S1L1}^2 = D_1 \times \left[I_{OL1}^2 + \frac{\Delta I_{OL1}^2}{12} \right], \quad I_{S1C1}^2 = D_{12} \times \left[I_{OC1}^2 + \frac{\Delta I_{OC1}^2}{12} \right],\tag{10}
$$

where (D_1) indicates the "ON" time of switch (S_1) , (D_{12}) represents the capacitor (C_1) discharged time at (D_1) , (I_{OL1}) and (I_{OC1}) stand for the inductor and capacitor current at the beginning. Then (ΔI_{OL1}) and (ΔI_{OC1}) stand for the respective average ripple current of inductor and capacitor as expressed in Eq. (11):

$$
\Delta I_{OL1} = \frac{I_{OL1-max} - I_{OL1-min}}{2} = \frac{10.7 - 0}{2} = 5.35,
$$
\n
$$
\Delta I_{OC1} = \frac{I_{OC1-max} - I_{OC1-min}}{2} = \frac{9.5 - 0}{2} = 4.75,
$$
\n(11)

where $(I_{OL1-max})$, $(I_{OL1-min})$ represents the maximum and minimum amplitude of inductor (L_1) current. In the same way ($I_{OCL-max}$), ($I_{OCL-min}$) represents the maximum and minimum amplitude of capacitor (C_1) current as illustrated in Fig. 9. It is evidently noticed from Fig. 10, that $D_1 = 0.3$, $D_{12} = 0.2$, $I_{OL1} = 0$, $I_{OC1} = 0$, $\Delta I_{OL1} = 5.35$ and $\Delta I_{OL1} = 4.75$. These values are substituted in Eq. (10) and Eq. (9), and the total current conduction and conduction loss of BB switch (S_1) as resolved in Eq. (12):

$$
I_{S1}^{2} = \left\{ D_{1} \times \left[I_{0L1}^{2} + \frac{\Delta I_{0L1}^{2}}{12} \right] \right\} + \left\{ D_{12} \times \left[I_{0C1}^{2} + \frac{\Delta I_{0C1}^{2}}{12} \right] \right\},
$$
\n
$$
I_{S1}^{2} = 0.713 + 0.368 = 1.0811 \text{ A}, \quad P_{cond-S1} = 1.0811 \times 0.07 = 0.075 \text{ W.}
$$
\n(12)

2.2.2.2. Turn-on and turn-off losses of switch (S_1)

Turn-on losses are defined to be an exposure of the component to a considerable amount of voltage and the current experienced simultaneously when the device turned on. In the same way, turn-off losses can also be defined to be an exposure of the component to a considerable amount of voltage and the current simultaneously experienced when the device is turned-off. Switching losses are produced as a consequence of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) simultaneously getting exposed to a high voltage and current while a transition happens between the open and the closed states. Hence it is enough to know about the duration and the kind of a transition, for instance resistive or inductive. The electrical characteristics of switch IRFZ24N ($t_r = 34$ ns, $t_f = 27$ ns, $V_{D-S1} = 18$ V) are utilized for simulation study and calculation of theoretical efficiency. The Turn-on and Turn-off of S_1 Losses ($P_{Turn-51}$) is computed by Eq. (13):

$$
P_{Turn-S1} = \frac{1}{2} \left(t_r + t_f \right) \times I_{S1}^2 \times V_{D-S1} \times F_{sw}, \ P_{Turn-S1} = 0.003 \text{ W}, \tag{13}
$$

where t_r is Rise time, t_f is Fall time, I_{s1}^2 refers to Current conduction of switch (S_1) (refer Eq. (12)), V_{D-S1} stands for drain voltage of switch (S_1) and, F_{sw} is operating switching frequency (5 kHz).

The total power losses of switch (S_1) is expressed in Eq. (14):

 $PL_{S1} = P_{cond-S1} + P_{Turn-S1}$, $PL_{S1} = 0.075 W + 0.003 W = 0.078 W.$ (14)

2.2.3. Calculation of losses in power sharing switching (S_2) in DOBB converter

2.2.3.1. Conduction loss of switch (S_2)

To analyze the conduction loss of S_2 , the device is simplified to be a stable voltage drop that is in in series with a linear resistor (RDS on = 0.07). RDS on is based on the applied VGS and the junction temperature. The conduction loss of switch (S_2) is expressed in Eq. (15):

$$
P_{cond-S2} = I_{S2}^2 \times RDS \text{ on } I_{S2}^2 = D_2 \times \left[I_{OS2}^2 + \frac{\Delta I_{OS2}^2}{12} \right],\tag{15}
$$

where (I_{52}) indicates the current flowing through the switch (S_2) , (D_2) stands for the "ON" time of switch (S_2), (I_{OS2}) represents the switch (S_2) current at time of starting, and (ΔI_{OS2}) stands for the average ripple current of switch (S_2). The switch current at the beginning instant ($I_{0.052}$) is derived from Eq. (16):

$$
I_{0S2} = I_{0S2 - min} + \Delta I_{0S2} = 7.565. \tag{16}
$$

The average ripple current (ΔI_{OS2}) is observed from Eq. (17):

$$
\Delta I_{OS2} = \frac{I_{OS2-max} - I_{OS2-min}}{2} = \frac{8.53 - 6.6}{2} = 0.965,\tag{17}
$$

where $(I_{0.52-max})$, $(I_{0.52-min})$ represents maximum and minimum amplitude of switch (S_2) current as illustrated in Fig. 10. It is seen from Fig. 11, that $D_2 = 0.22$, $I_{0.052} = 7.565$ and $\Delta l_{0.052} = 0.965$, which are substituted in Eq. (15), the total current conduction and conduction loss of power sharing switch (S_2) as resolved in Eq. (18):

$$
I_{S2}^2 = 12.6 \text{ A}, \ P_{cond-S2} = 12.6 \times 0.07 = 0.88 \text{ W}. \tag{18}
$$

Fig. 11. Representation of key waveform during switch (S_2) conduction

2.2.3.2. Turn-on and turn-off losses of switch (S_2)

The electrical characteristics of switch IRFZ24N ($t_r = 34$ ns, $t_f = 27$ ns, $V_{D-S2} = 34$ V) are utilized for the purposes of simulation studies and calculation of theoretical efficiency. The switch (S_2) Turn-on and Turn-off losses ($P_{Turn-52}$) is computed by Eq. (19):

$$
P_{Turn-S2} = \frac{1}{2} (t_r + t_f) \times I_{S2}^2 \times V_{D-S2} \times F_{sw}, \ P_{Turn-S2} = 0.134 \text{ W}, \tag{19}
$$

where I_{52}^2 refers to current conduction of switch (S_2) (refer Eq. (18)), V_{D-S2} is: drain voltage of

switch (S_2) and F_{sw} is Operating switching frequency (10 kHz)

The total power losses of switch (S_2) is obtained from Eq. (20):

$$
PL_{S2} = P_{cond-S2} + P_{Turn-S2}, PL_{S2} = 0.88 W + 0.134 W = 0.93 W.
$$
\n(20)

2.3. Loss of diode (D_1) in DOBB converter

For the diode (D_1), the loss due to forward voltage ($V_{F_1} = 0.8$) is expressed by Eq. (21):

$$
PL_{D1} = I_{D1} \times V_{F1}, \quad I_{D1} = D_{d1} \times \left[I_{OD1}^2 + \frac{\Delta I_{OD1}^2}{12} \right],
$$
\n⁽²¹⁾

where (I_{D1}) indicates the current flow through the diode (D_1) , (D_{d1}) stands for the "ON" time of diode (D_1) , (I_{OD1}) refers to the diode (D_1) current at the time of starting and (ΔI_{OD1}) stands for the average ripple current of diode (D_1) . The diode current at the beginning instant (I_{OD1}) equals to zero, therefore the average ripple current (ΔI_{OD1}) is obtained from Eq. (22):

$$
\Delta I_{OD1} = \frac{I_{OD1-max} - I_{OD1-min}}{2} = \frac{6.5 - 0}{2} = 3.25,\tag{22}
$$

where $(I_{OD1-max})$, $(I_{OD1-min})$ indicates the maximum and minimum amplitude of diode (D_1) current as illustrated in Fig. 11. It can be seen clearly from Fig. 12, that $D_{d1} = 0.15$, $I_{0.01} = 0$ and $\Delta l_{OD1} = 3.25$. These values are substituted in Eq. (21), the total current conduction and the power loss of diode (D_1) as resolved in Eq. (23):

$$
I_{D1} = 0.132 A, PL_{D1} = 0.132 \times 0.8 = 0.1 W.
$$
\n(23)

2.4. Loss of diode (D_2) in DOBB converter

For the diode (D_2), the loss due to forward voltage ($V_{F2} = 0.8$) is provided by Eq. (24):

$$
PL_{D2} = I_{D2} \times V_{F2}, \quad I_{D2} = D_{d2} \times \left[I_{OD2}^2 + \frac{\Delta I_{OD2}^2}{12} \right],
$$
\n(24)

where (I_{D2}) indicates the current flow through the diode (D_2) , (D_{d2}) stands for the "ON" time of diode (D_2), (I_{OD2}) refers to the diode (D_2) current at the time of starting, and (ΔI_{OD2}) stands for the average ripple current of diode (D_2) . The diode current at the instant (I_{OD2}) of starting equals to zero, hence the average ripple current (ΔI_{OD2}) is derived from Eq. (25):

$$
\Delta I_{OD2} = \frac{I_{OD2-max} - I_{OD2-min}}{2} = \frac{9.5 - 0}{2} = 4.75. \tag{25}
$$

where $(I_{OD2-max})$, $(I_{OD2-min})$ represent the maximum and minimum amplitude of diode (D_2) current as illustrated in Fig. 13. It is observed from Fig. 12 that $D_{d2} = 0.19$, $I_{OD2} = 0$ and $\Delta I_{OD2} = 4.75$. These values are substituted in Eq. (24), the total current conduction and the power loss of diode (D_2) as is done in Eq. (26):

$$
I_{D2} = 0.36 \text{ A}, \quad PL_{D2} = 0.36 \times 0.8 = 0.29 \text{ W}.
$$
\n
$$
(26)
$$

2.5. Loss of inductor (L_1) in DOBB converter

Losses in an inductor are contributed by two factors. One factor is the wire loss and the second one is the core loss. The loss because of the wire is provided by Eq. (27):

$$
PL_{L1} = I_{L1}^2 \times R_{dcl1}, \quad I_{L1}^2 = D_{L1} \times \left[I_{0L1}^2 + \frac{\Delta I_{0L1}^2}{12} \right],\tag{27}
$$

where (I_{L1}) stands for the current flow through the inductor (L_1) , $(D_{L1} = D_1 + D_2 + D_{d1})$ indicates the "ON" time of inductor (L_1) , (I_{OL1}) refers to inductor (L_1) current at time of starting, $(R_{dcl1} = 0.9)$ stands for the equivalent dc resistance of 0.1 mH Ferrite core inductor and (ΔI_{OL1}) refers to the average ripple current of inductor (L_1) .

The inductor current at the instant of starting (I_{0L1}) equals to zero, therefore the average ripple current (ΔI_{OL}) is observed from Eq. (28):

$$
\Delta I_{OL1} = \frac{I_{OL1-max} - I_{OL1-min}}{2} = \frac{10.5 - 0}{2} = 5.25.
$$
\n(28)

where $(I_{0L1-max})$, $(I_{0L1-min})$ represent the maximum and minimum amplitude of inductor (L_1) current as illustrated in Fig. 14. shows clearly that $D_{L1} = 0.67$, $I_{OL1} = 0$ and $\Delta I_{OL1} = 5.25$. These values are substituted in Eq. (27), the total current conduction and power loss of inductor (L_1) are resolved in Eq. (29):

$$
I_{L1}^2 = 1.538 \text{ A}, \quad PL_{L1} = 1.538 \times 0.9 = 1.384 \text{ W}.\tag{29}
$$

2.6. Total power losses in DOBB converter

The total power losses in DOBB converter is the summation of all the factors mentioned above. The total power losses (T_L) and system efficiency can be calculated making use of Eq. (30):

$$
T_L = PL_{S1} + PL_{S2} + PL_{D1} + PL_{D2} + PL_{L1} = 2.782 \text{ W}, \text{Efficiency} = \frac{P_{DOBB}}{P_{DOBB} + T_L},\tag{30}
$$

where, P_{DOBB} is Output power of DOBB converter (40 W) and T_L refers to total power losses

3. Results and discussion

To find out the performance of the proposed converter under the present control strategy, MATLAB simulations in different conditions with symmetrical and asymmetrical output voltage variation have been performed.

The simulation parameters such as input voltage (V_{in}) , input current (I_{in}) , first output voltage, current and power of DOBB converter $(V₀₁, I₀₁$ and $P₀₁)$ respectively, second output voltage, current and power of DOBB converter (V_{02} , I_{02} and P_{02}) respectively and total output voltage (V_T) and total power (P_T) are used to evaluate the performance of the proposed system as shown in Table 1.

Table 1. Shhahahon bahamolors for DODD converter			
Components and symbols	Parameters		
Input inductor (L_1)	389.4 µH		
Intermediate capacitor (C_1)	$50 \mu F$		
Output capacitors (C_1 and C_2)	1000 µF, 100 V		
Operating switching frequency (F_{sw}) of switches	$S_1 = 5$ kHz, $S_2 = 10$ kHz		
Load resistances $(R_1$ and R_2)	28.8Ω		

Table 1. Simulation parameters for DOBB converter

3.1. Symmetrical output voltage control of DOBB converter

To verify the symmetrical performance of DOBB converter, input dc voltage source is considered as $(V_{in} = 18 \text{ V})$ as shown in Fig. 15(a). The output voltages of the DOBB converter are desired to be regulated on $(V_{01} = 24 \text{ V}$ and $V_{02} = 24 \text{ V}$). Consequently, the total output voltage and total power are desired to be regulated on $(V_T = 48 \text{ V})$ and $(P_T = 40 \text{ W})$. Moreover, load resistances ($R1 = R2 = 28.8 \Omega$) are considered for symmetrical condition.

Fig. 15. Performance of DOBB converter under symmetrical voltage condition

In Figs. 15(c) and (d), output voltages (V_{01} and V_{02}) are shown. As seen from this figure, the output voltages are tracked with the references values (V_{01}^* and $V_{02}^* = 24$ V) with minimum steady state error. It is obvious that the output voltages are regulated very well. Similarly, the currents $(I₀₁$ and $I₀₂$) drawn from load resistances $R₁$ and $R₂$ are shown in Figs. 15(e) and (f), both the loads consume 20 W power from input supply individually. Therefore, the power drawn from load resistances R_1 and R_2 are shown in Figs. 15(g) and (h). In Fig. 15(i), the total output voltage $(V_T = V_{01} + V_{02})$ and total output power $(P_T = P_{01} + P_{02})$ are shown. As seen from this figure, voltage and power are tracked with the reference values ($V_T^* = 48$ V and $P_T^* = 40$ W). It is obvious that the output voltage and power are regulated smoothly. Thus, the 40 W loads draw current from input dc source as is revealed in Fig. 15(b).

Fig. 16. Output voltage ripple evaluation of proposed DOBB converter

Moreover, two different switching frequencies of switches ($S_1 = 5$ kHz and $S_2 = 10$ kHz) are desired to be separate the inductor discharging current as three portions. The top and bottom portion of inductor current i_{L_1} , energies the output capacitor (C_{Q_2}) . The middle portions of inductor current i_{L1} , energies the output capacitor (C_{01}). Thus, it will reduce the output ripple considerably as shown in Fig. 16. Moreover, switching losses and conduction losses of switch S_1 and $S₂$ are analysed with respective switching frequency and duty cycle as shown in Fig. 17. The switching frequency of the solid-state switches is kept on the order of $S_1 = 5$ kHz, $S_2 = 10$ kHz for proper operation. Such high switching frequency causes high switching losses in the switch S_2 .

Fig. 17. Analysis of losses in switches S_1 and S_2 with respective switching frequency and duty cycle

3.2. Simulated comparison of two conventional converter with the proposed DOBB

To identify the limitations of conventional converters Nami et al. [7] and Boora et al. [8], the output voltages of the conventional converters are desired to be regulated on $(CO_1 = 24 \text{ V}, CO_2 = 24 \text{ V}$ i.e. $V_T = 48 \text{ V}$ from 0 to 0.4 Sec. After 0.4 sec, the output voltages are desired to be regulated on $(V_{01} = 18 \text{ V}, V_{02} = 30 \text{ V}$ i.e. $V_T = 48 \text{ V}$) respectively as shown in Figs. 18 and 19. For this analysis input dc voltage source is considered to be 18 V and load resistances are considered to be $R_1 = R_2 = 28.8$ OHM.

Fig. 18. Figure performance of Nami et al. (2010) converter when $V_{01} < V_{02}$

Fig. 19. Performance of [8] converter

Observing from Figs. 18 and 19 conventional converters [7, 8] output voltages ($CO₁ = 24$ V, $CO_2 = 24$ V i.e. $V_T = 48$ V) are regulated very well at symmetrical condition. But in asymmetrical condition, which is $V_{01} < V_{02}$, not able to follow the output voltage as proved. Because the output capacitor ($CO₁$) has the individual charging ability but another capacitor ($CO₂$) does not have the individual charging ability. Alternatively, the proposed DOBB converter has the individual charging ability of both capacitors ($CO₁$, $CO₂$). Therefore, DOBB converter follows the reference voltages at both symmetrical and asymmetrical conditions as shown in Fig. 20.

Fig. 20. Performance of DOBB converter

Converter presented by						
Switching states		States of output capacitors				
S ₁	S_{2}		CO.	\mathcal{C}_{O2}		
	0		Discharge	Discharge		
$\overline{0}$	0		Charge	Charge		
0			Charge	Discharge		
Converter presented by [8]						
	Switching states		States of output capacitors			
S ₁	S_2	S_3	CO.			
$\overline{0}$	0	0	Charge	Charge		
$\overline{0}$	0	1	Charge	Discharge		
0		θ	Discharge	Discharge		
	0	1	Charge	Discharge		
	θ	$\overline{0}$	Charge	Charge		
		0	Discharge	Discharge		
Proposed DOBB converter						
Switching states		States of output capacitors				
\mathcal{S}_1	S,		CO.			
$\overline{0}$			Charge	Discharge		
	0		Discharge	Charge		
$\overline{0}$	0		Charge	Discharge		

Table 2. Voltage control ability of conventional and proposed converters

The voltage control ability of conventional and proposed converters is estimated using Table 2. It is obvious from the table that in [7] the output voltage (CO_2) is greater than (CO_1) the reason is that the output capacitor $(CO₁)$ has the individual charging ability at switching states $(0, 1)$, but the output capacitor (CO_2) does not have the individual charging ability at all the three switching states, therefore second output voltage $(CO₂)$ always depends on first output voltage $(CO₁)$. Similarly, in the study by [8] the output capacitor $(CO₁)$ has the individual charging ability at switching states $(0, 0, 1)$ and $(1, 0, 1)$. But the output capacitor $(CO₂)$ does not have the individual charging ability at all the six switching states, therefore second output voltage (CO_2) always depends up on the first output voltage $(CO₁)$. Moreover, in [8] not able to control the output voltage (CO_2) is greater than (CO_1) but in DOBB converter the output capacitors (CO_1) and (CO_2) have the individual charging ability at switching states $(0, 1)$ and $(1, 0)$ respectively. It is one of the main advantages of the proposed DOBB converter.

The proposed DOBB converter topologies are compared with respect to their component count, type of conversion, possibility of output voltage control, switching states and driver circuit complexity. Table 3 presents a comparison between topologies of interest. It should be noted that the converter presented by [7] has the lowest number of semiconductor devices in the current conduction path. However, it has three main disadvantages: a step-up conversion is only possible, the second output voltage ($CO₂$) always equal/lesser than the first output voltage ($CO₁$), and separate grounding of switches leads to an individual power supply for driver circuit. Similarly, the converter presented by [8] has three main disadvantages: a higher component count, the second output voltage ($CO₂$) is always equal/lesser than the first output voltage ($CO₁$) and separate grounding of switches. Finally, these disadvantages can be minimized by implementing DOBB converter which has many advantages: step-up and step-down conversions are possible, lower component count and both the output capacitor voltages (VO_1 or $VO_2 < V_t$) is controllable. Further common grounding switches present in DOBB converter reduces power supply, noise emission problems and improves the efficiency of it.

Table 3. Performance comparison of the conventional and proposed DOBB converters with various objects

Various dual output converters			
Converter presented	Converter presented	Proposed DOBB	
by $\sqrt{7}$	by [8]	converter	
∍			
	(Both step-up and	(Both step-up and	
	step-down)	step-down)	
Simple	Complex	Simple	
Medium	Complex	Simple	
	Total number of components (Step-up) Switching states complexity		

3.3. Algorithm of repetitive control and feedforward compensation control

The repetitive compensator is the compensator which adds the input signal to the output one which delays the input one by only one cycle Tr . In this research, in order to realize the repetitive compensator by DSP, we have to design it by the discrete system. Fig. 5 shows the fundamental operation of the repetitive compensator and the time leading element in the discrete system. As shown in Fig. 5, the repetitive compensator consists of N memories, and in the case the control period is T', and the relation of $Tr = NT'$ is derived. As this control system, in the case the period of the input signal (ripple torque) Tr synchronizes with the rotation speed of the brushless DC motor, the number of N also change with change of Tr , in the system fixed the control period T' inconveniently. Then, T' is allowed to change and the repetitive compensator with N memories in one period Tr is realized by synchronizing the control period T' with the rotation angle of the rotor *gre.* The input signal to the repetitive compensator ($=$ the output signal from the proportional compensator) is averaged within the period of T' and added to the data in the corresponding memory.

3.4. Experimental results of the proposed DOBB

For verifying the efficiency of the system proposed, a low power range laboratory prototype is constructed as illustrated in Fig. 21. For the experimental arrangement, two diverse input power sources are used. A power supply with the electric specification of 18 V, 2.386 A and 42.96 W, are considered to be the input power source. The prototype parameters of proposed system are given in Table 5.

Fig. 21. Prototype model of proposed DOBB converter system

3.5. Performance of C_{01} capacitor

The input voltage (230 V) is step down to (18 V) using the transformer and converted to DC with the help of bridge rectifier and the input is fed to controller with the help of voltage regulator. The output voltage from controller is given to enhanced converter unit and the output voltage across the individual capacitor c_{01} is displayed using the DSO. Fig. 22 shows the output waveform of the C_{01} capacitor.

3.6. Performance of C_{02} capacitor

The input voltage (230 V) is step down to (18 V) using the transformer and converted to DC with the help of bridge rectifier and the input is fed to controller with the help of voltage regulator. The output voltage from controller is given to enhanced converter unit and the output voltage across the individual capacitor c_{02} is displayed using the DSO. Fig. 23 shows the output waveform of the C_{02} capacitor.

3.7. Performance of switch S_1 in boost mode

Fig. 24 shows the output waveform of PWM Pulses across the switches S_1 in the Boost mode. These PWM pulses are generated by driver circuit by means of the mode selection switches connected along with the microcontroller.

Fig. 22. C_{01} output voltage waveform of DOBB converter: a) simulation b) experimental waveform

Fig. 23. C_{02} output voltage waveform of DOBB converter: a) simulation, b) experimental waveform

Fig. 24. Boost voltage waveform of DOBB converter: a) simulation, b) experimental waveform PWM pulses across the switch S_1 in boost mode

3.8. Performance of switch S_1 in buck mode

Fig. 25 presents output Pulses across the switches S_1 in the Buck mode. These PWM pulses are generated by driver circuit by means of the mode selection switches connected along with the microcontroller.

Fig. 25. Buck voltage waveform of DOBB converter: a) simulation, b) experimental waveform PWM pulses across the switch S_1 in buck mode

3.9. Performance of switch S_2 in boost mode

Fig. 26 shows the output Pulses across the switches S_2 in the Boost mode. These PWM pulses are generated by driver circuit by means of the mode selection switches connected along with the microcontroller.

Fig. 26. Boost voltage waveform of DOBB converter: a) simulation, b) experimental waveform PWM pulses across the switch S_2 in boost mode

3.10. Performance of the switch S_2 **in buck mode**

Fig. 27 presents the output Pulses across the switches S_2 in the Buck mode. These PWM pulses are generated by driver circuit by means of the mode selection switches connected along with the microcontroller.

Fig. 27. Buck voltage waveform of DOBB converter: a) simulation, b) experimental waveform PWM pulses across the switch S_2 in buck mode

4. Conclusions

In this paper, a new structure of DOBB and frequency components of vibrations has been proposed. The proposed topology extends the design flexibility and the possibility to optimise the

power converter for achieving the main objectives. Compared with conventional inverter systems, the proposed system is employed with reduced voltage stress, reduced switch count and DC source count. The proposed DOBB configuration required at least two DC sources for Converter Exhaustive operations are carried out, switching losses are calculated, simulation results are carried out for symmetrical and asymmetrical output voltage. The proposed DOBB Converter is compared with the conventional one and finally, it is proved to be more efficient than the other conventional converters. In addition, the proposed methods were examined in the case of low speed drive of the brushless DC motor. However, for the higher order frequency components of the vibration and those near the sharp resonance frequency of the mechanical system, the effectiveness of the proposed vibration suppression method was small. Several analyses in terms of cost, semiconductor loss and harmonics have been made and it is inferred that the proposed structure can be an appropriate aspirant for power converters used in industrial and drive applications.

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