2873. FPGA based quasi z-source cascaded multilevel inverter using multicarrier PWM techniques

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Abstract. FPGA based Quasi Z-Source Cascaded Multilevel Inverter (Quasi Zs-CMLI) using multicarrier PluseWidth Modulation (PWM) techniques are presented in this paper. Multicarrier based PWM techniques have been proposed for seven level Quasi Zs-CMLI and implemented using Field Programmable Gate Array (FPGA). For generating gating pulses to the inverter switches, Phase Disposition (PD), Inverted Phase Disposition (IPD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) techniques are programmed on FPGA. In the proposed system, three solar PV emulator modules are used. These are acting as input source to the inverter. Finally, THD comparison made between different carrier based modulation with shoot through and non-shoot through the states. The proposed quasi Zs-CMLI and PWM techniques are verified through MATLAB/Simulink. For confirmation of simulation results, A laboratory prototype model have been implemented using FPGA. The capture hardware results are matched with simulation results.

Keywords: multicarrier PWM techniques, quasi Z-source MLI, solar PV emulator, shoot through control and FPGA control.

Nomenclature

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AC	Alternating current
APOD	Alternative phase opposition disposition
CMLI	Cascaded multilevel inverter
EMI	Electromagnetic interference
FPGA	Field programmable gate array
IPD	Inverted phase disposition
MATLAB	Matrix laboratory
NST	Non-shoot through
PD	Phase disposition
POD	Phase opposition disposition
PV	Photovoltaic
Quasi Zs-CMLI	Quasi z-source cascaded multilevel inverter
ST	Shoot through
THD	Total harmonic distortion

1. Introduction

In recent years, Multilevel inverters(MLIs) have drawn tremendous interest in the area of high voltage and high-power applications along with renewable energy sources such as wind energy systems, Photovoltaic (PV) systems, Fuel cell etc. MLIs having numerous features such as low distortion output waveform, reduced voltage stress, reduced EMI, operate with lower switching frequency and higher efficiency [1]. MLIs are classified into three types, they are (i) Diode

clamped MLIs (ii) Flying capacitor MLIs (iii) Cascaded MLIs. Among the MLIs, the cascaded MLI structure is well suited for a PV system, but it has some own drawbacks like three stage power conversion, lower efficiency and short circuit problem. To overcome the drawbacks of conventional inverter, Z-source inverter have been presented in this paper [2]. The Zs-CMLI uses the LC impedance network to connect a DC voltage source to the inverter [3, 4]. The Z-source inverter translate the zero state of traditional inverter into a shoot-through (short circuit) states, thereby achieving the buck/boost of the input DC source. The Z-source inverter structure has several advantages as compared to traditional inverter, including lower costs, single stage conversion and more reliable. Even though, Z-source inverters suffer from the drawback of discontinuous input current that lead to very high harmonics. So that the impedance network is modified to form the quasi Z-source inverter that has continuous input current with reduction in voltage rating of impedance network [4-8]. The Quasi Zs-CMLIs are mainly used in the photovoltaic power generation system that has advantage of balanced DC-link voltage control, distributed maximum power tracking, modular structure and reduced AC side filter requirements. These features cannot be realized in traditional CMI. There are several multicarrier based PWM techniques used to control the output voltage of traditional MLI. The multicarrier PWM can be implemented with less complexity, offers better performance in all the operating conditions and also allow the over modulation region [7-10]. The contribution of this papers: Six different carrier based PWM techniques such as triangular, sawtooth, unipolar, sine(regular), stepped wave and staircase with four modulation schemes (PD, IPD, POD and APOD) are implemented for Quasi Zs-CMLI. In this work, the emulator has been used as input to the Quasi Zs-CMLI. The performance of multicarrier techniques are analysed in terms of THD % profile with a different modulation index and effect of the carrier wave on the shoot-through state also analysed. The prototype model of the proposed system has been implemented using FGPA and tested with different modulation schemes for the seven level quasi under ST and NST conditions.

2. Quasi Z-source inverter

The single phase quasi Z-source inverter circuit is shown Fig. 1(a). This inverter consists of quasi Z-source along with a normal H bridge inverter. Quasi Z-source consists of two inductors (L_1 and L_2– 2 mH), two capacitors (C_1 and C_2– 3300 mF) and diode. Normal H-bridge inverter consists of four MOSFETs (S_1, S_2, S_3 and S_4). The Quasi Zs-CMLI operates at two modes of operation, namely: Non-Shoot Through(NST) mode and Shoot-Through (ST) mode.
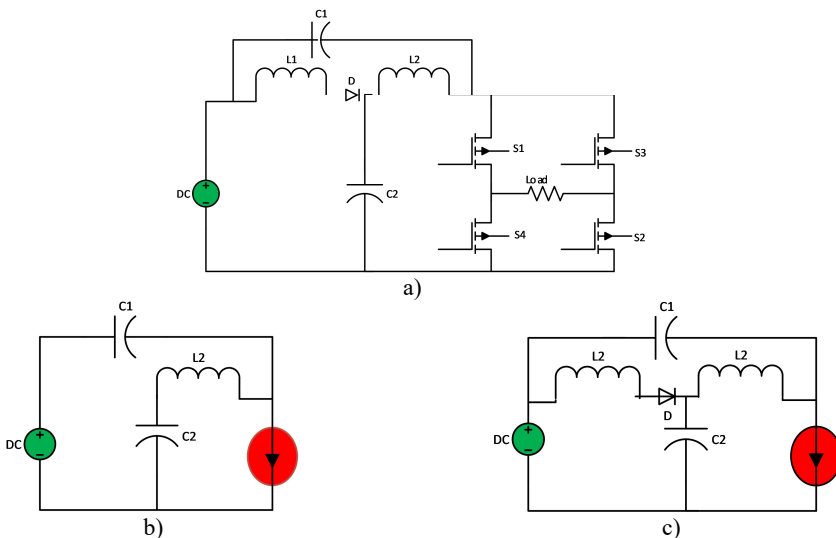
Fig. 1. Circuit diagram, 1: a) single stage quasi Z-source b) quasi at ST mode 1, c) quasi at NST mode

The equivalent circuit of ST and NST modes are shown in Fig. 1(b) and 1(c) respectively. In NST mode, Quasi Zs-inverter operate as a normal traditional inverter and its operate at active state. The capacitor C_1 is charged to the input voltage and C_2 charged to voltage across the L_2, the voltage across the inductor (V_{L1}, V_{L2}), capacitor(V_{C1}, V_{C2}) and $V_{dc-link}$ are expressed as:

$$V_{L1} = V_{dc} - V_{C1}, \quad V_{L2} = -V_{C2}, \tag{1}$$
$$V_{dc-link} = V_{C1} - V_{L2} = V_{C1} + V_{C2}, \quad V_d = 0. \tag{2}$$

Assume T_S is total switching period, which is an inversion of switching frequency f_s, T_{ST} is the shoot-through period and T_{NST} is non-shoot through the period.so that $T_S = T_{ST} + T_{NST}$. Fig. 1(a)-(c). shows equivalent circuits of single stage quasi, ST and NST conditions. In ST mode, Quasi Zs-inverter operates as a buck/boost converter and it operates at zero state. The diode is reverse biased due to capacitor voltage V_{C1} exceeds the input voltage. Now, C_1 is discharged through L_2 and input current continue to flow through L_1 and C_2. After ST mode, the energy transferred to the inductance is added to the normal state and hereby boosted voltage is obtained. The average inductor voltage V_{L1} and V_{L2} over the switching cycle is zero. The average capacitor voltage is expressed as:

$$V_{C1} = \frac{T_{NST}}{T_{NST} - T_{ST}} V_{dc}, \tag{3}$$
$$V_{C2} = \frac{T_{ST}}{T_{NST} - T_{ST}} V_{dc}. \tag{4}$$

The DC-link voltage can be derived by substituting Eqs. (3) and (4) in Eq. (2):

$$V_{dc-link} = V_{C1} + V_{C2} = \frac{T_S}{T_{NST} - T_{ST}} V_{dc} = \frac{1}{1 - 2\frac{T_{ST}}{T_S}} V_{dc}, \tag{5}$$

where, B is the boost factor of Quasi Zs-CMLI. The Quasi Zs-CMLI are highly suited for PV systems, individual PV emulators can be connected at each H-bridge input. Each H-bridge inverter produce three level output, namely $+V_{DC}$, 0 and $-V_{DC}$. The output load voltage has a number of levels equal to $2n + 1$ where n is the number of input DC sources.

3. Seven level quasi Z-source cascaded multilevel inverter

Fig. 2. Shows the power circuit diagram of proposed FPGA based quasi Z-source CMLI topology where each H-bridge has LC impedance and impedance network fed from the individual PV emulators.

**Table 1.** Switching states of seven-level quasi Z-source Inverter

Voltage level	Output voltage	State	On switches
Level 1	+3VDC	Active state	S1, S2, S5, S6, S9, S10
Level 2	+2VDC	Active state	S1, S2, S5, S6, S9, S11
Level 3	+1VDC	Active state	S1, S2, S5, S7, S9, S11
Level 4	0	Zero state	S4, S2, S8, S7, S12, S10
Level 4	0	Shoot-through state	S1 To S12
Level 5	–VDC	Active state	S3, S4, S6, S8, S10, S12
Level 6	–2VDC	Active state	S3, S4, S7, S8, S10, S12
Level 7	–3VDC	Active state	S3, S4, S7, S8, S11, S12

The switching states of Quasi Zs-CMLI are shown in the Table 1. In each active state, six switches have in 'ON state' and other switches been in 'OFF position'. During zero state, all the

switches are turned to 'ON state' for the boost operation of quasi network. The switching states of seven level Quasi Zs-CMLI shown in the Table 1.

4. Multicarrier based sine pulse width modulation techniques

In this paper, six multicarrier based SPWM techniques combined to shoot-through state and simple boost technique developed for Quasi-CMI as follows: Triangular (TMC), Saw Tooth (STMC), Unipolar Sine (UPMC), Sine (Regular) (SMC), Stepped (SPMC) and Staircase (SCMC). Multicarrier PWM techniques entail the natural sampling of a single modulating or reference waveform typically being sinusoidal same as that of output frequency of the inversion system, through several carrier signals.
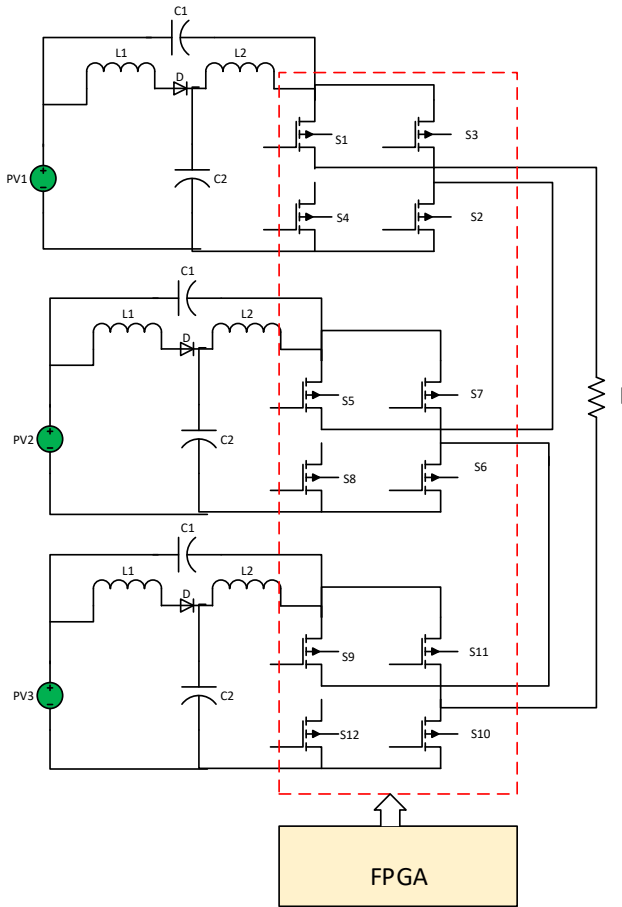
Fig. 2. FPGA-based seven level quasi Z-source CML

There are different scheme of switching techniques have been proposed for controlling of multilevel inverters. There are two types of carrier based PWM are i) Phase shifted carrier PWM and Carrier disposition PWM. Further, Carrier disposition PWM classified into Alternate Phase opposition disposition (APOD), Phase Opposition Disposition (POD) and Inverse Phase Disposition (IPD). In the PD switching methods, (M-1) the carrier signals have same phase and frequency. APOD Switching methods is very similar to PD but only difference is each carrier signals phase shifted by 180° from the adjust carrier. In this control technique, most of the harmonics are appeared at around the carrier frequency. In the phase opposition methods, (M-1) carrier signals are required to generate gating pulses for the N level inverter and upper half of the
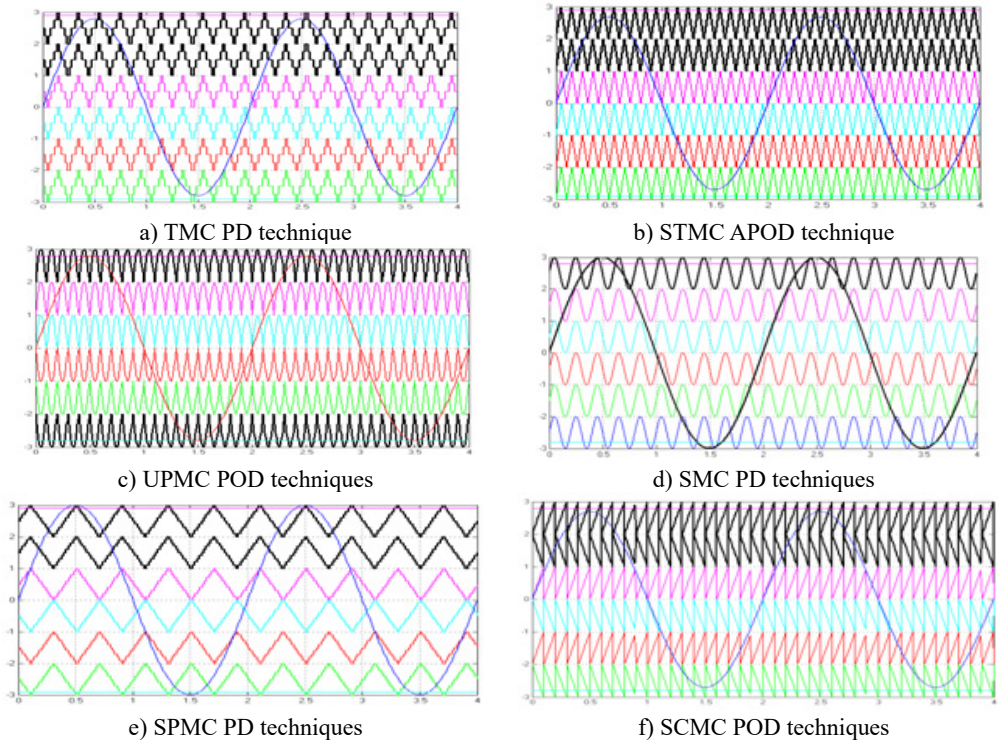
two signals are in same phase and lower half will be 180° out of phase with upper half. In the IPD PWM approach the level shifted carrier signal are 180° out of phase when compared to the PD. These carrier signals are compared with a sinusoidal modulating wave. The reference or modulation waveform has peak amplitude A_m and frequency f_m, and it is centered in the middle of the carrier set. If the reference is greater than the carrier signal, then the active device corresponding to that carrier is switched ON, and if the reference is less than the carrier signal, then the active device corresponding to that carrier is switched OFF. The carrier frequency defines the switching frequency of the converter. Modulation index of multilevel inverters is defined as:

$$M_a = \frac{A_r}{\left(\frac{m-1}{2}\right) * Ac},$$

(6)

where, A_r and A_c are the amplitude of the reference and the carrier signal respectively.

5. Simulation results

The seven level quasi Z-source inverter has been simulated using MATLAB/SIMULINK. The PD, IPD, POD, and APOD modulation schemes are used for the six multicarrier SPWM techniques. The operating frequency of the Quasi Zs-CMLI is 5 kHz where as 1 kHz to 10 kHz switching frequency used in the existing literature. The inverter gives poor THD performance at lower operating frequency while inverter offers good performance at higher frequencies (10 kHz). However, higher frequency of operation will lead to higher switching losses. Hence, 5 kHz switching frequency has been chosen in this proposed work. The THD performances of the proposed system have been evaluated and compared with all modulation techniques. These modulation strategies are implemented and illustrated from Figs. 3(a)-3(f).

a) TMC PD technique

b) STMC APOD technique

c) UPMC POD techniques

d) SMC PD techniques

e) SPMC PD techniques

f) SCMC POD techniques

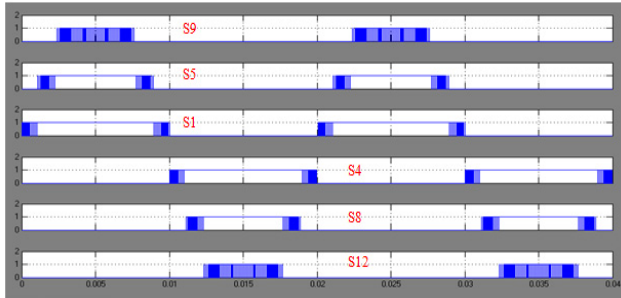**Fig. 3.** Simulation waveforms for multicarrier SPWM techniques

Fig. 4. Switching pulse with shoot through ratio $D_0 = 10$ % and modulation index $M_a = 0.9$
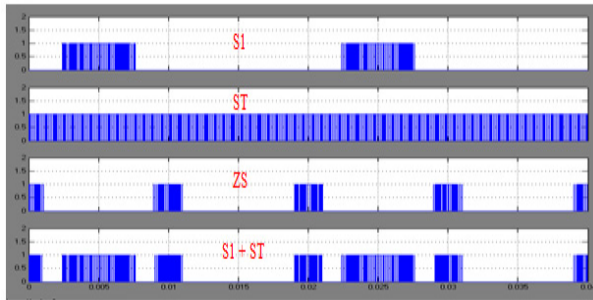

Fig. 5. S1: Switching pulse for S1 switch, ST: Shoot-through pulse, ZS: Zero state, S1+ST: S1 pulses combined with ST wave
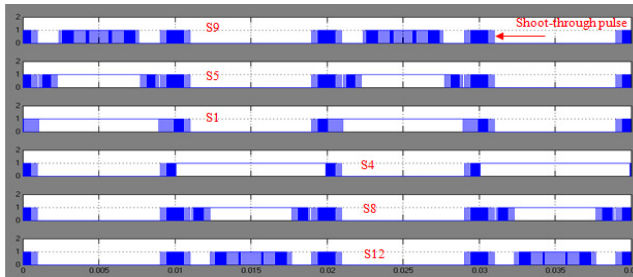

Fig. 6. Switching pulse with shoot through ratio $D_0 = 90$ % and modulation index $M_a = 0.9$

The switching pulses are generated from simulation and shown in Figs. 4-6. The output voltage and harmonic spectrum of proposed system are obtained for fundamental frequency with different duty ratio. The MATLAB simulation has been carried for duty ratio of 10 % and Modulation index $M_a = 0.9$ and duty ratio of 90 % and Modulation index $M_a = 0.9$. Here, only presents, duty ratio of 90 % and Modulation index $M_a = 0.9$. Table 2 shows the fundamental load voltage and load voltage THD % for the six carriers with shoot through ratio 90 % and modulation index 0.9. The Quasi Zs-CMI operate as a boost converter. The boost factor is set as $B = 2$. The seven level output voltage obtained are approximately 0, ±90 V, ±180 V and ±270 V.

From Table 1, it is observed that, the TMC POD and TMC PD methods provide almost equal to the calculated value. However, TMC APOD PWM gives minimum (i.e. boost factor compared to the other modulation within TMC PWM methods). In all available literature, the boost factor is derived only for the triangular carrier waveform. This paper analyses the effect of another carrier waveform. From the simulation results, it is inferred that, stepped carrier (PD, APOD modulation) and staircase carrier (PD, APOD modulation) achieved the maximum boost. In terms of % THD, SMC PWM gives a minimal voltage and current THD of 9.17 % and 8.96 % compared to the other methods. The load voltage, load current waveform (RL load- 20 Ohms, 1 mH) and corresponding

harmonic spectrum are shown in the Figs. 7 to 10 respectively. Figs. 11 and 12 show the output load voltage value against % THD respectively. The fundamental load current and load current THD % are given in the Table 3.

Table 2. Output load voltage %THD for Seven-Level Quasi-CMI with shoot-through ratio = 90 %
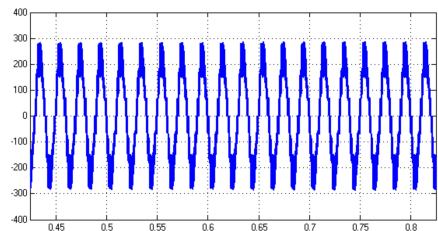
	Load voltage %THD											
	Shoot-through ratio = 90 %											
	TMC		STMC		UPMC		SMC		SPMC		SCMC	
SPWM modulation	Volt V)	THD (%)	Volt V)	THD (%)	Volt V)	THD (%)	Volt V)	THD (%)	Volt V)	THD (%)	Volt V)	THD (%)
PD	266.00	12.19	266.00	12.61	231.1	10.27	230.30	9.52	320.20	17.85	312.80	18.53
IPD	252.60	12.64	266.80	10.46	207.00	13.78	227.70	9.17	254.10	13.80	279.80	17.27
POD	273.00	13.44	279.40	11.44	303.00	14.36	229.10	9.31	320.20	17.85	312.80	18.53
APOD	245.00	11.86	234.00	09.57	209.10	15.91	228.10	9.42	254.10	13.34	279.70	17.35

Table 3. Output load current %THD for Seven-Level Quasi-CMI with shoot-through ratio = 90 %

|	Load current % THD											
	Shoot-through ratio = 90 %											
	TMC		STMC		UPMC		SMC		SPMC		SCMC	
SPWM modulation	Amp (A)	THD (%)	Amp (A)	THD (%)	Amp (A)	THD (%)	Amp (A)	THD (%)	Amp (A)	THD (%)	Amp (A)	THD (%)
PD	13.30	11.98	14.00	12.76	13.09	10.06	13.00	9.30	16.01	14.75	15.64	15.64
IPD	12.63	12.46	13.34	10.29	10.36	13.59	12.76	8.96	12.7	11.93	13.99	14.41
POD	13.65	13.24	13.97	11.30	7.094	7.49	12.9	9.09	16.01	14.75	15.64	15.64
APOD	12.22	11.66	11.69	9.67	10.45	15.72	12.8	9.6	12.71	11.49	13.98	14.50
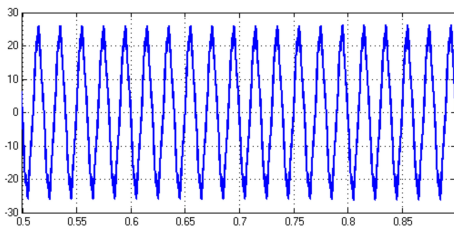
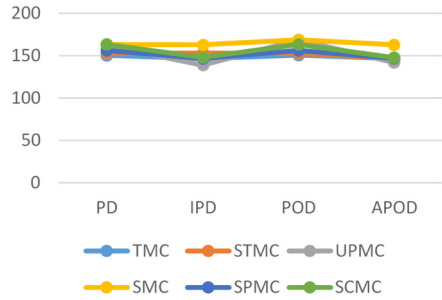**Fig. 7.** Load voltage

Fig. 8. Load current
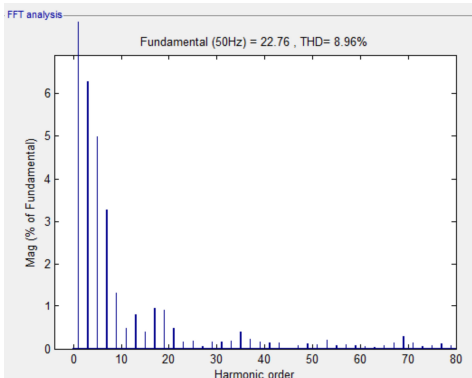
Fig. 9. Voltage harmonics spectrum
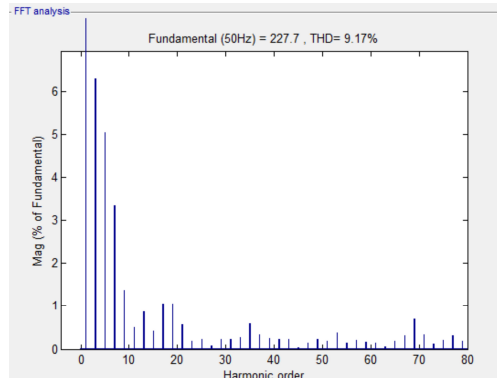
**Fig. 10.** Current harmonics spectrum
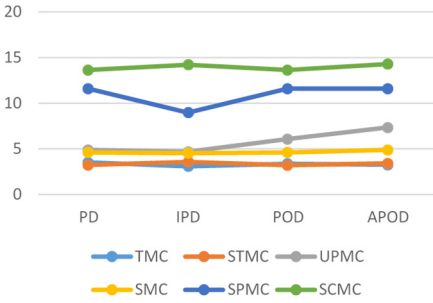
Fig. 11. Load voltage THD % shoot through ratio $D_0 = 90$ % and Modulation index $M_a = 0.9$

Fig. 12. Load voltage value shoot through ratio $D_0 = 90$ % and Modulation index $M_a = 0.9$

6. Hardware results

The Quasi Zs-CMLI using multicarrier PWM techniques has been implemented using the FPGA based prototype model. It consists of three quasi Z-source network, PV Emulator, three full H-bridge, load and FPGA-Spartan-6 controller. The switching pulses generated from FPGA are shown in Figs. 13-15.
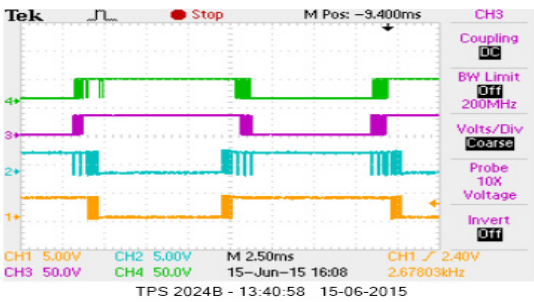
Fig. 13. Switching Pulse for S1, S2, S3 and S4 with shoot through ratio $D_0 = 90$ % and modulation index $M_a = 0.9$
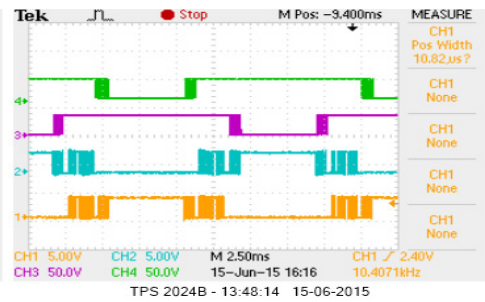
Fig. 14. Switching pulse for S5, S6, S7 and S8 with shoot through ratio $D_0 = 90$ % and modulation index $M_a = 0.9$
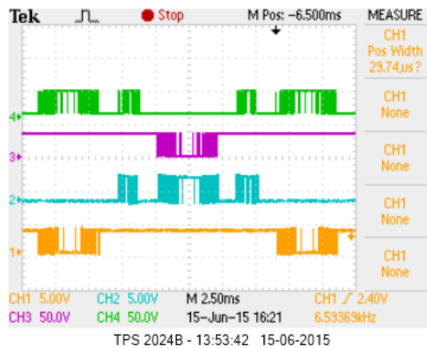

Fig. 15. Switching pulse for S9, S10, S11 and S12 with shoot through ratio $D_0 = 90$ % and modulation index $M_a = 0.9$

The prototype model of the proposed system has been designed using IRF250N MOSFETs and IN5408 diodes. In this hardware setup, three Solar PV Emulators are used which acting as input DC source (20V) for the Quasi Zs-CMLI. The impedance network consists of 4700 µf capacitors and 2 mH inductors. The SPWM switching signals are generated with help of Spartan-6 (XC6SLX9) FPGA controller. The generated switching signals are interfaced to the inverter power

switches through driver TLP250. The switching frequency is 5 KHz. The hardware results are captured using Fluke power spectrum analyser and measured gating pulses are shown in Figs. 13, 14 and 15 respectively. The experimental results of seven-level output voltage and current waveform are shown in Figs. 16 and 17for $D_0 = 10$ % and 90 %, respectively.The experimental voltage and current harmonics are shown in the Figs. 18 and 19. The THD % obtained from experimental method is 4 % at $D_0 = 10$ % for TMC SPWM techniques which is below the IEEE standards. Table 4 shows the comparison of simulation and hardware results. From Table 4, it is observed that simulation results are good agreement with hardware results.
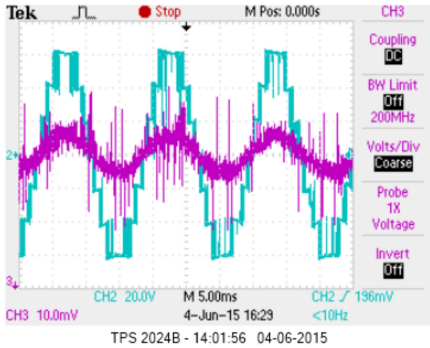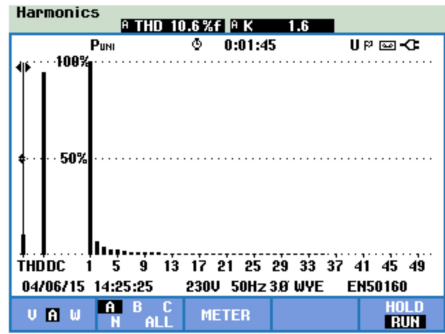

Fig. 16. Load voltage and current for shoot-through ratio $D_0 = 10$ % and modulation index $M_a = 0.9$ (CH 2:20V/DIV, 5 ms/DIV
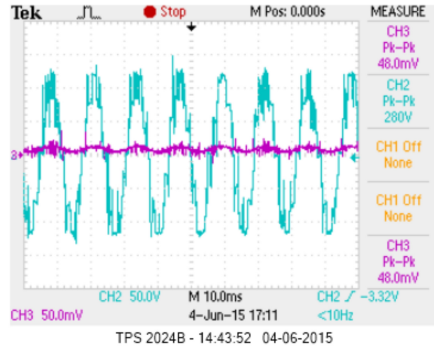
Fig. 17. Load voltage and current for shoot-through ratio $D_0 = 90$ % and modulation index $M_a = 0.9$ (CH 2:50V/DIV, 10 ms/DIV)
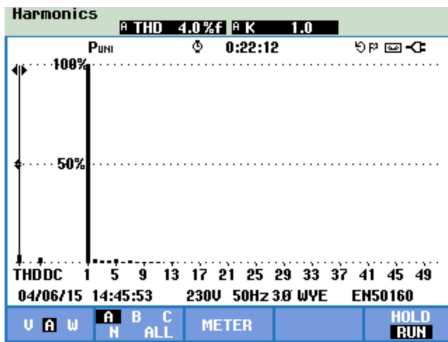
Fig. 18. Load voltage harmonic spectrum at $D_0 = 10$%

Fig. 19. Load voltage harmonic spectrum at $D_0 = 90$ %

Table 4. Comparison of simulation and hardware results

Input voltage (V)	Boost factor	Output voltage (V) $D_0 = 10$ %	Output voltage (V) $D_0 = 90$ %	Output voltage THD %	
				$D_0 = 10$ %	$D_0 = 90$ %
Simulation $V_{dc} = 20$ V	2	60 V	140 V	2.89	12.01
Experiment $V_{dc} = 20$ V	2	60 V	140 V	4.00	10.60

7. Conclusions

In this work, multicarrier based SPWM techniques with different duty ratio has been implemented using FPGA for seven-level Quasi Zs-CMLI. The THD profile and voltage boost capability of the proposed system has been analysed and compared with duty ratio of 10 % and 90 % respectively. From the analysis, it is observed that phase opposition disposition (POD) Sine-Regular multicarrier technique offers the minimal voltage THD of 4 % for shoot through duty ratio of 10 % over other modulation and PWM techniques. The simulation results of proposed

seven-level Quasi Zs-CMLI has been validated through FPGA controller based prototype model. The boosted voltage and percentage THD profile obtained from the prototype model are in good agreement with the simulation results.

Acknowledgements

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